JWH7232

802.3af Compliant PD interface with High Efficiency Flyback Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H7232 is an integrate IEEE 802.3af PoE complaint Powered Device (PD), it includes PD interface and high efficiency flyback controller.
The JWH7232 has all the functions of IEEE 802.3af, including detection, classification, power up inrush and operation current limit as well as a Hot-swap MOSFET.

The DCDC converter uses primary-side regulation without opto-coupler feedback, simplifying the system design. It also supports secondary-side feedback design.

The JWH7232 is available in a space-saving 28-pin QFN (4mm × 5mm) package.

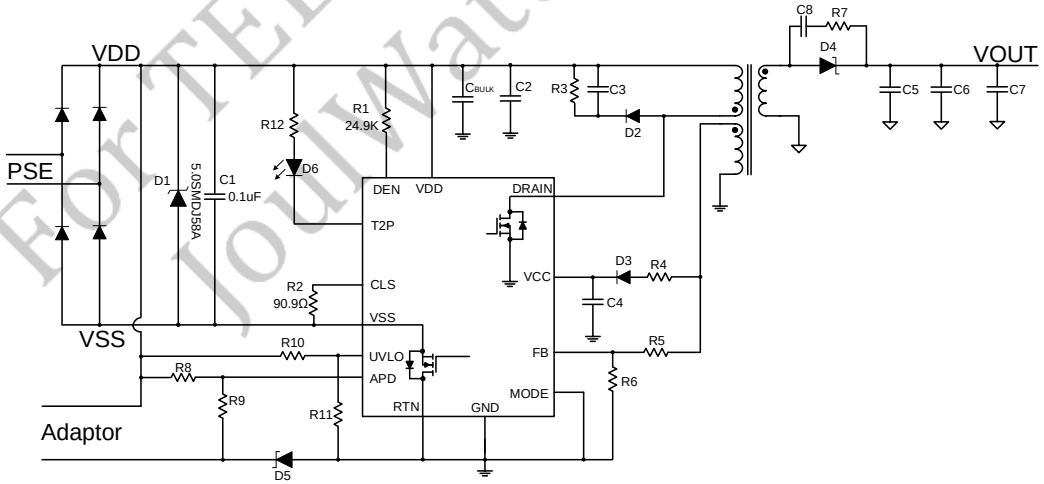
FEATURES

- Compatible with IEEE 802.3af specifications
- Integrate 100V PD hot-swap MOSFET
- Auxiliary adaptor oring power Supply
- Support multiple topology design
  Primary-side regulated flyback
  Secondary-side regulated flyback
- Output diode compensation in PSR mode
- Up to 500kHz adjustable switching frequency
- Hiccup protection for OLP, OVP and thermal shutdown
- EMI reduction with frequency dithering
- Available in 28-pin QFN 4mm × 5mm-28 package

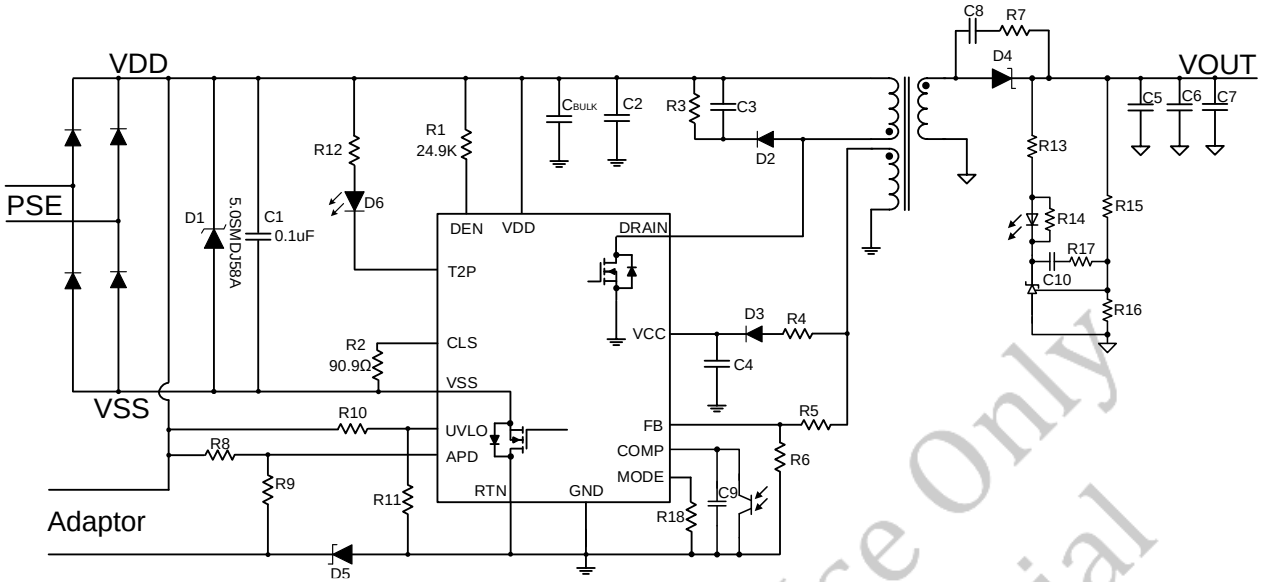
APPLICATIONS

- IEEE 802.3af-compliant devices
- Security camera
- WLAN access points
- IoT devices

TYPICAL APPLICATION



PSR typical application



SSR typical application

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWH7232QFNU#TR	QFN4*5*0.85-28	JWH7232 YW□□□□□	Green

Notes:

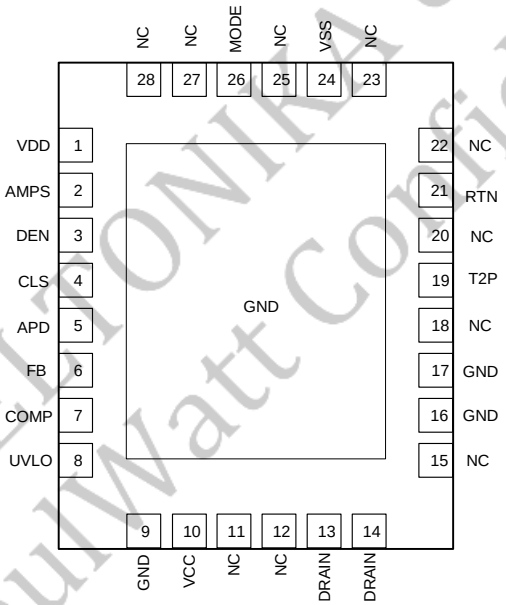
1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- Joulwatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING1）

Pins Voltage Respects to VSS:

VDD, RTN, DEN, T2P, APD, GND……-0.3V to 100V

AMPS……-0.3V to 100V

CLS……-0.3V to +6.5V

Pins Voltage Respects to GND:

VDD ……-0.3V to 100V

DRAIN ……-0.3V to 200V

FB, COMP……-0.7V to 100V

VCC ……-0.3V to 20V

MODE, UVLO……-0.3V to +6.5V

Pins Voltage Respects to VDD:

APD ……-6.5V to +0.3V

Pins Current:

T2P Sinking Current……10mA

VCC Sinking Current……1.5mA

APD Sinking Current……-5mA

FB Sinking Current……±2mA

Junction Temperature[2) 3)]……150ºC

Lead Temperature (Soldering, 10 sec)……260ºC

Storage Temperature…… -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

Supply Voltage VDD……0V to 57V

Switching Voltage V_{DRAIN}……-0.5V to 150V

Maximum T2P Sinking Current……5mA

Maximum VCC Sinking Current……1.2mA

Maximum APD Sinking Current……-3mA

Maximum FB Sinking Current……±0.5mA

Maximum Switching Frequency……500kHz

Maximum Switching Current Limit……3A

Operating Junction Temperature……-40ºC to 125ºC

ELECTROSTATIC DISCHARGE RATING

Human Body Model (HBM)……±2kV

Charged Device Model (CDM)……±500V

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{JC}
QFN4x5-28……	40ºC/W	9ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH7232 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD, CLS, DET, APD, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND, GND and RTN are shorted together. The ● denotes the specifications which apply over the full operating temperature range(-40°C to 125°C), otherwise specifications are at T_A=25 ℃. VDD-VSS=48V, VSS=0V, and R_{DEN}=24.9KΩ, R_{CLS}=41.2Ω, unless otherwise noted.

Item	Symbol	Condition			Min.	Typ.	Max.	Units
Detection								
Detection on	V_{DEN_ON}	V_{DD} rising				1.2	1.6	V
Detection off	V_{DEN_OFF}	V_{DD} rising				12		V
DET Leakage Current	V_{DEN_LK}	V_{DET}=V_{DD}=57V, Measure I_{DET}				0.1	1	uA
Bias Current		V_{DD}=10.1V, float DEN pin, not in Mark event, Measure I_{SUPPLY}				5	12	uA
Detection current	I_{DEN}	V_{DD}=1.6V, Measure I_{SUPPLY}				64		uA
		V_{DD}=10.1V, Measure I_{SUPPLY}				410		uA
Classification								
Classification Stability Time[5)]	t_{SETUP}					150		uS
Classification Voltage	V_{CLASS}	13V<V_{DD}<21V 1mA<I_{CLASS}<43mA				2.5		V
Classification Current	I_{CLASS}	13V<V_{DD}<21V, Guaranteed by V_{CLASS}, not tested in production						
		R_{CLASS}=1270Ω, 13V<V_{DD}<21V				2		mA
		R_{CLASS}=243Ω, 13V<V_{DD}<21V				10.55		mA
		R_{CLASS}=137Ω, 13V<V_{DD}<21V				18.7		mA
		R_{CLASS}=90.9Ω, 13V<V_{DD}<21V				28.15		mA
		R_{CLASS}=62Ω, 13V<V_{DD}<21V				41		mA
		R_{CLASS}=0Ω, 13V<V_{DD}<21V				60		mA
Classification Mark Threshold	V_{Mark_th}	V_{DD} rising				12		V
		V_{DD} falling				11.2		V
Classification Upper Threshold	V_{CLSOFF}	V_{DD} rising				22		V
Classification Reset Threshold	V_{Reset_th}	V_{DD} falling				5		V
Mark Event Current	I_{MARK}					1.5		mA
Mark Event Resistance	R_{MARK}						12	kΩ
IC Supply Current during Classification	I_{IN_CLASS}					40	100	uA
Class Leakage Current	I_{LKG}	V_{CLS}=0V, V_{DD}=57V,					1	uA
PD UVLO								
VDD Turn on Threshold	V_{ON}	V_{DD}-V_{SS} rising				35		V

VDD Turn off Threshold	V_{OFF}	V_{DD}-V_{SS} falling			31		V
IC Supply Current during Operation[5)]	I_{IN}	V_{DD}-V_{SS}=57V			450		uA
Pass Device and Current Limit							
On Resistance[5)]	R_{ON_RTN}	I_{RTN}=600mA			0.48		Ω
Leakage Current	I_{RTN_LKG}	V_{DD}=V_{RTN}=57V			1	15	uA
Current Limit	I_{LIM}	V_{RTN}=1V			530		mA
Inrush Current Limit	I_{INRUSH}	V_{RTN}=2V			130		mA
Inrush Current Termination[5)]		V_{RTN} falling			1.2		V
Inrush to Operation Mode Delay	T_{DELAY}				115		mS
AMPS							
Maintain Power Signature Current Threshold	V_{MPS}	R_{MPS}=100Ω, 37V<V_{DD}<57V			24		V
Maintain Power Signature Current Limit	I_{MPS_LIM}	R_{MPS}=0Ω, 37V<V_{DD}<57V			25		mA
Auto MPS falling Current threshold					42		mA
	Hysteresis				2		mA
Maintain Power Signature Duration	T_{MPS}				100		mS
Maintain Power Signature Period	T_{MPDO}				180	240	mS
T2P							
T2P Output Low Voltage		V_{T2P}=2mA, respect to VSS			0.1	0.3	V
T2P Output High Leakage Current		V_{T2P}=48V				1	uA
APD							
APD High Threshold Voltage	V_{APD_H}	VDD-APD			1.5		V
APD Low Threshold Voltage	V_{APD_L}	VDD-APD			1		V
APD Leakage Current		VDD-APD=5V				2	uA
VDD UVLO for APD Detection[5)]	V_{DD_UVLO}	rising			7.5		V
		falling			5.5		V
Protection							
Short circuit protection threshold[5)]	V_{SC}				20		V
Short circuit protection deglitch time[5)]	t_{SC}				0.5		uS
Short circuit protection recover time[5)]	t_{SCR}					10	uS
Over current protection threshold[5)]	V_{LIM}				10		V
Over current protection deglitch time[5)]	t_{OC}				1.2		mS
Thermal Shut down Temperature[5)]	T_{PD_SD}				155		°C

Thermal Shut down Hysteresis[5)]	T_{PD_HYS}				20		°C
Adaptor detection deglitch time[5)]	t_{APD}				10		mS
PD turn on deglitch time[5)]	t_{PDON}				150		uS
PD turn off deglitch time[5)]	t_{PDOFF}				10		uS
State Machine deglitch time[5)]	t_{SM}				10		uS
Flyback Part							
VDD Section (VDD Pin)							
Supply current from VDD pin	I_{HV}	VDD=12V, VCC=0V			5		mA
Leakage current of VDD pin	I_{VDD_LK}	VDD=57V, VCC=20V			20		uA
VDD UVLO Section (UVLO Pin)							
VDD UVLO Threshold	V_{UVLO_ON}	V_{UVLO} rising			1.2		V
UVLO Pin Floating Detection Current	I_{UVLO_DET}				5		uA
UVLO Blanking Time	T_{UVLO_BLK}	$V_{UVLO}=V_{UVLO\_ON}$-0.4V		0.5		1	us
Supply Voltage Section (VCC Pin)							
Turn-On Threshold Voltage	V_{CC_ON}	VCC Rising, TA = 25°C			8		V
Turn-Off Threshold Voltage	V_{CC_OFF}	VCC Falling, TA = 25°C			5.5		V
Threshold Voltage for Latch Release	V_{CC_DLH}				4.5		V
Startup Current	I_{CC_ST}	VCC=VCC_ON-0.5 V, TA = 25°C			80		uA
Operating Supply Current	I_{CC_OP}	VCC=6 V, C_{DRV}=1nF, fs=500kHz			1.5		mA
VCC OVP Clamp Current	I_{VCC_OVP}				5		mA
VCC OVP Voltage	V_{CC_OVP}				16		V
VCC OVP Blanking Time	$T_{VCC\_OVP\_BLK}$				100		us
Working Mode Programming Section (MODE Pin)							
Mode Pin Source Current	I_{MODE}				40		uA
SSR Detection Threshold	V_{SSR}				0.15		V
Voltage Sense Section (FB Pin)							
Maximum FB Source Current Capability	I_{FB_MAX}				2		mA
FB Reference	V_{FB_REF}				1.2		V

Output OVP threshold	V_{FB_OVP}				1.45		V
Output OVP Debounce Cycle Counts	N_{VS_OVP}				3		Cycle
Output OVP Hiccup Off Time	T_{OVP_HIC}				60		ms
Current Sense Section (CS Pin)							
Maximum Switching Current Limit	I_{SW_max}				2.5		A
Minimum Switching Current Limit	I_{SW_min}				0.6		A
Leading-Edge Blanking Time	t_{LEB}				150		ns
Primary side SCP	I_{SCP}				3		A
Frequency Jittering Section							
Peak Jittering Amplitude to FB					±7%		
Peak Jittering Frequency	f_{PK_JIT}				33		kHz
Frequency Jittering Amplitude					±7%		
Jittering Frequency	f_{JIT}				200		Hz
DRV Section *(DVR Pin)*							
Maximum ON Duty	D_{ON_MAX}				70		%
Minimum ON Time	T_{ON_MIN}				150		ns
Maximum OFF Time	T_{OFF_MAX}				40		us
Maximum Switching Frequency	f_{max}	Constant in PSR or SSR, R_{MODE}=7.5kΩ			500		kHz
		SSR, R_{MODE}=37.5kΩ			100		kHz
Minimum Switching Frequency	f_{min}				30		kHz
COMP Section (COMP Pin)							
Soft Start Time	T_{SS}				12		ms
Open Pin Voltage	V_{COMP_MAX}	Open Loop			2.5		V
Internal Pull-Up Resistor	R_{COMP_UP}				10		kΩ
OLP Hiccup On Time[5)]	T_{OLP_ON}				6		ms
OLP Hiccup Off Time[5)]	T_{OLP_OFF}				60		ms
Internal Over Temperature Protection							
Thermal Shutdown	T_{OTP}				150		°C

Threshold[5)]							
OTP Hysteresis[5)]	T_{HYS}				30		ºC

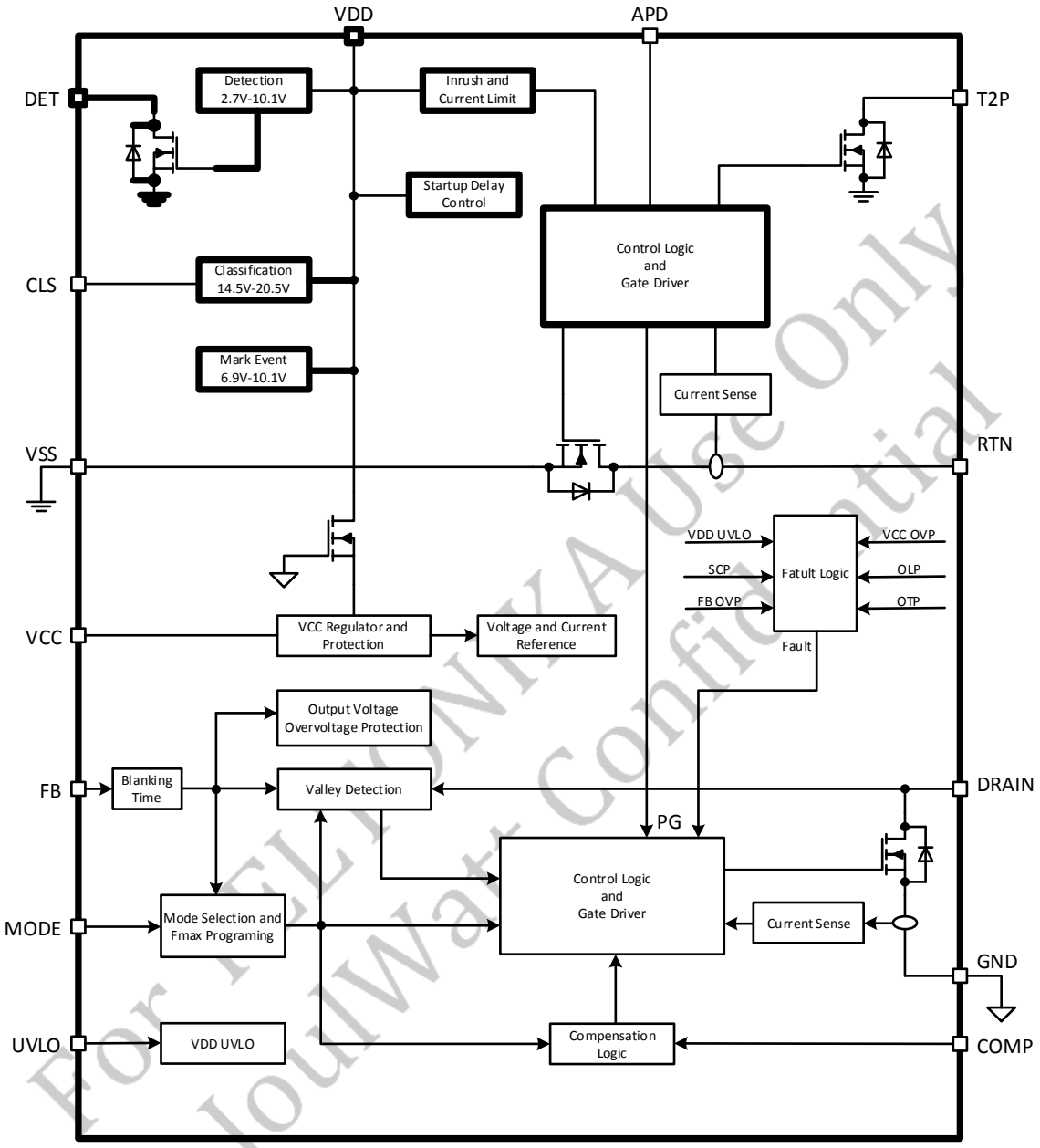
Note：

5) Guaranteed by design, not subject to test.

PIN DESCRIPTION

Pin	Name	Description
1	VDD	Positive power supply terminal from PoE input power rail.
2	AMPS	Connect resistor from AMPS to VSS to program MPS current.
3	DEN	Connect a 24.9kΩ resistor between VDD and DEN for PoE detection.
4	CLS	Connect resistor from CLS to VSS to program classification current.
5	APD	Auxiliary power input detector. Use this pin for adaptor supply application. When the voltage of VDD-APD is higher than V_{APD_H}, the hot-swap MOSFET and CLS pin function is disabled, and the JWH7232 force T2P and PG active.
6	FB	Feedback pin for fly-back solution.
7	COMP	External compensation pin for SSR solution.
9, 16, 17	GND	Power Ground for fly-back circuit.
10	VCC	Supply bias voltage pin, powered through internal LDO from VIN. It is recommended to connect a 1uF capacitor between VCC and GND.
8, 11, 12, 15, 18, 20, 22, 23, 25, 27, 28	NC	No connection.
13,14	DRAIN	Internal fly-back MOSFET drain.
19	T2P	Type 2 PSE indicator, open drain output. Pulled low to VSS indicates the presence of a Type 2 PSE or APD is enabled. High impedance indicates a Type 1 PSE or no input.
21	RTN	Drain of PD hot-swap MOSFET, connect GND to this pin.
24	VSS	Negative power supply terminal from PoE input power rail.
26	MODE	PSR and SSR mode select pin.
29	GND	Exposed pad, connected to GND.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

TA = +25°C, unless otherwise noted

TBD

PD FUNCTIONAL DESCRIPTION

The JWH7232 is an integrate IEEE 802.3af PoE complaint Powered Device (PD), it includes PD interface and high efficiency flyback converter.

The JWH7232 PD interface has all the functions of IEEE 802.3af, including detection, classification, power up inrush and operation current limit as well as 100V Hot-swap MOSFET.

Compared with IEEE 802.3af, the IEEE 802.3at standard establishes a higher power allocation for PoE while maintaining the compatibility with the IEEE 802.3af systems. Power Sourcing Equipment (PSE) and Powered Device (PD) are defined as Type 1 complying with the IEEE 802.3af, or Type 2 complying with the IEEE 802.3at. the standard establishes a method of communication between PSE and PD with detection, classification and mark event.

The JWH7232 is one integrated PD solution with IEEE 802.3af PD interface and 13W DCDC converter.

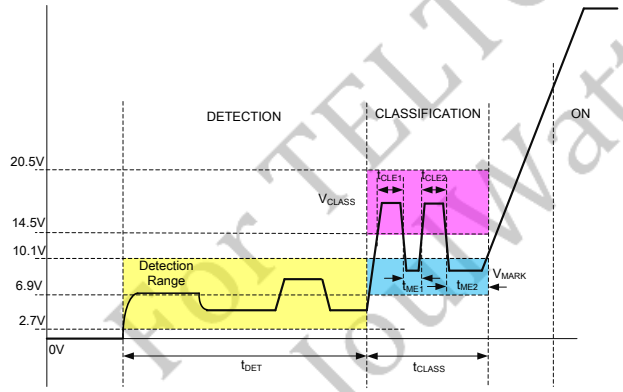


Figure 1. PD Interface Operation Description (2-Event Classification)

Detection

The R_{DET} connected between DET and VDD pin is presented as a load to the PSE in Detection Mode, when the input voltage is between 2.7V to 10.1V, the DET pin is pulled down to VSS and R_{DET} (24.9KΩ±1%) is connected as the load of PSE. The detection resistance seen from PI is the result of the input bridge resistance in series with the VDD loading. The input bridge resistance is partially cancelled by JWH7232 effective leakage resistance during detection.

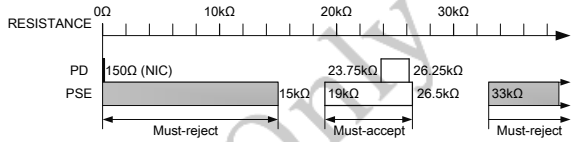


Figure 2. IEEE 802.3af Signature Resistance Ranges

Classification

802.3af Classification

A PD can optionally present a classification signature to the PSE to indicate the maximum power it will draw while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V), with the current level indicating one of 5 possible PD classes. Figure 4 shows a typical PD load line, starting with the slope of the 25kΩ signature resistor below 10V, then transitioning to the classification signature current (in this case, Class 3) in the V_{CLASS} range.

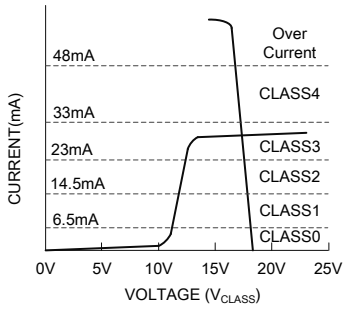


Figure 3. PD Classification

JWH7232 presents a current in classification

mode as showing in Table 1.

Table 1. CLASS Resistor Selection

Class	Max. Input Power to PD (W)	Classification Current (mA)	R_{CLASS}(Ω)
0	12.95	2-	1270
1	3.84	10.6	243
2	6.49	18.7	137
3	12.95	28.2	90.9
4	25.5	40.4	62

PD Interface UVLO and Current Limit

When PD is powered by PSE and V_{DD} is higher than turn on threshold, the Hot-swap switch will turn on with a limited current I_{INRUSH} to charge the downstream DCDC input capacitor C_{BULK}. The startup charging current is around 120mA.

After the t_{DELAY} from UVLO starting, if RTN voltage drops to lower than 1.2V, Hot swap current limit will change to 530mA and the JWH7232 will assert PG signal and go from the startup mode to the running mode, the PG signal can enable downstream DCDC converter internally.

If V_{DD} drops below UVLO, the Hot-swap MOSFET and the DCDC converter both are disabled.

If output current is equal or higher than internal current limit, current limit loops works and V_{RTN} rise. when $V_{LIM}<V_{RTN}<V_{SC}$, the current limit timer starts counting, if the current limit timer expires, the current limit reverts to the inrush value, and PG is pulled down internally to disable DCDC regulator at the same time.

If $V_{RTN}>V_{SC}$, the internal circuit shutdown the hot-swap MOS and returns on the MOS, the current limit timer runs. When the current limit timer expires, the current limit reverts to the inrush value, and PG is pulled down internally to disable DCDC regulator at the same time.

Figure 4 Shows the current, PG and T2P work logic during startup from PSE power supply.

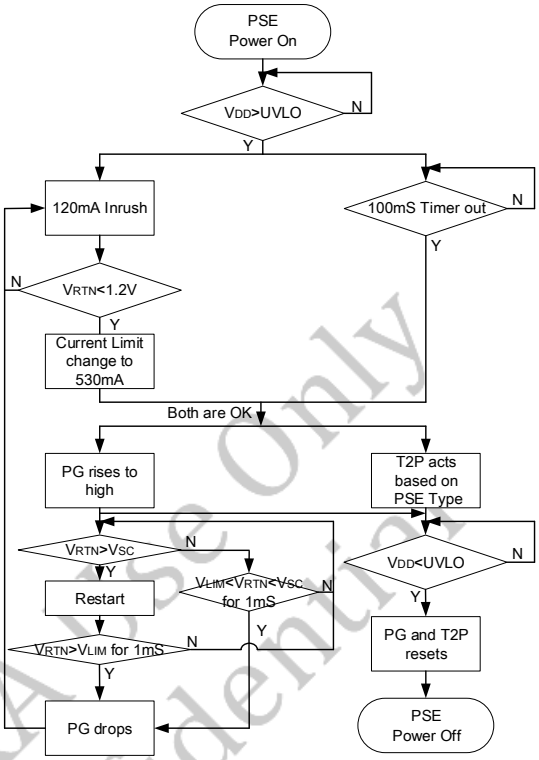


Figure 4. Startup Sequence

Maintain Power Signature

In order to maintain power, the JWH7232 provide a valid Maintain Power Signature (MPS) at the PI (Power Interface).

If the PD MOS current is less than 40mA, an internal MPS timer starts counting, when the PD MOS current is larger than 40mA for t_{MPS}, the MPS timer reset until the current is less than 40mA again.

When the timer is larger than t_{MPDO}, the timer reset and the AMPS pin output V_{MPS} voltage for t_{MPS}, the PI sinks the maintain current I_{MPS}.

Wall Power Adaptor Detection and Operation

For Applications where an auxiliary power

source such as a wall adaptor is used to power the device, the JWH7232 features wall power adaptor detection as showing in figure 5.

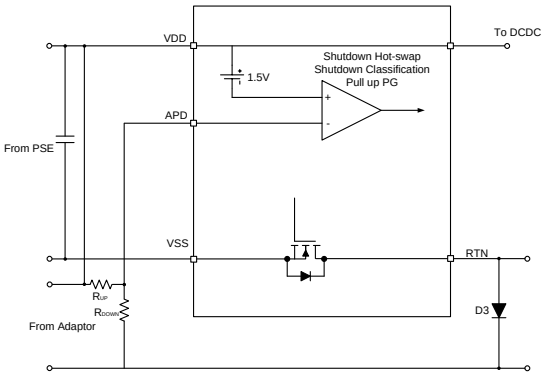


Figure 5. Adaptor Power Detection

There is a 1.5V reference voltage from V_{DD} to APD for adaptor detection. The adaptor is detected when APD voltage triggers:

V_{DD}-V_{APD}=V_{ADPTOR}*R_{UP}/(R_{UP}+R_{DOWN})>1.5V

If the adaptor voltage is much higher than the design adaptor voltage, VDD-VAPD will be high. If it is higher than 6.5V, the JWH7232 inner circuit will clamp the VDD-VAPD voltage at 6.5V, then a current will flow out through the APD pin, the current should be limited lower than 3mA by external resistor.

D3 is used to block reverse current between adaptor and PSE power source. When a wall adaptor is detected, the internal MOSFET between RTN and VSS turns off, classification current is disabled and T2P becomes active, the PG signal is active when adaptor is detected, so that it can enable the downstream DCDC converter even input hot-swap MOSFET is disabled.

T2P Indicator

The T2P signal is an open drain output. After t_{DELAY} from UVLO starting and RTN drops to 1.2V and a Type 2 PSE is detected, or a wall power adaptor is detected, the T2P signal will be pulled low to indicate a Type 2 PSE or an adaptor is detected.

Protection

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. JWH7232 has temperature monitor circuit for PD hot-swap MOSFET, when the PD temperature is higher than protection threshold, it will turn off the PD MOS and the PG signal is pulled low. The DCDC converter also stops working due to the PG signal is low.

When the temperature is lower than its recovery threshold, the chip is re-enabled and the PD MOS returns on slowly.

DC/DC FUNCTIONAL DESCRIPTION

Start-Up

VDD Start-Up

When PG is high, the internal JFET turns on and a VDD current source starts to charge VCC cap. As soon as the VCC voltage reaches turn-on threshold V_{CC_ON}, the controller is enabled and the converter starts switching. the internal startup circuit will be disabled when VCC reaches V_{CC_ON}.

Soft-Start

In the absence of a detected fault, the controller begins to work normally along with soft start. The internal soft-start time is within 12ms with the COMP voltage V_{COMP} rising gradually from the minimum level to the maximum level. Every restart up is followed by a soft start.

Normal Operation

After the controller start-up, it enters normal operation. There will be three working mode in JWH7232 for different application, SSR, PSR. The combination of resistor on MODE pin determines the working mode of JWH7232.

Working Mode Selection

At the initial 100us, the voltage on MODE pin and FB pin are detected to determine the working mode of the JWH7232. The default working mode is PSR mode. When PG is logical high and VCC reaches V_{CC_ON}, the MODE pin voltage V_{MODE} is sensed to be compared with a 150mV internal reference voltage. If V_{MODE} is greater than 150mV, the JWH7232 will work in SSR mode, otherwise it will work in PSR mode. Then the working mode will be locked until the next VCC UVLO reset.

At the same time, FB voltage is compared with a 2V reference voltage to determine the output voltage sensing method.

In PSR mode, the output voltage is sensed for OVP and valley detection. In one method, FB is coupled to an auxiliary winding through a resistor divider to abstract output voltage information from Vaux. The initial FB voltage will be much smaller than 2V. This means the JWH7232 will work in PSR mode.

In SSR mode, the output voltage is sensed only for OVP. If the OVP protection is unnecessary in some application, FB pin will be floating, an initial 2uA pull-up current will pull the FB pin voltage greater than 2V. Otherwise, FB will be coupled to an auxiliary winding through a resistor divider to abstract output voltage information for OVP. The initial FB voltage will be much smaller than 2V in this case.

Table 3. Working Mode Selection

Mode	Mode Pin Initial Voltage(mV)		FB Pin Initial Voltage(V)	
	Min.	Max.	Min.	Max
SSR	150	--	0	2
SSR without OVP	150	--	2	--
PSR	0	150	0	2

SSR Working Mode

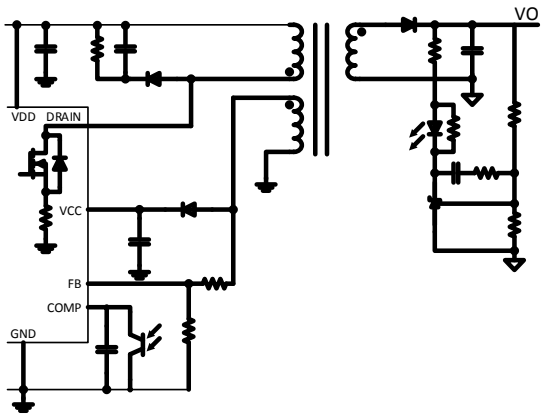


Figure 6. Typical application in SSR mode

In SSR working mode, the maximum switching frequency f_{SW} can be programed by the external resistance R_{MODE} at MODE pin. The relationship between f_{SW} and R_{MODE} is shown in figure 7.

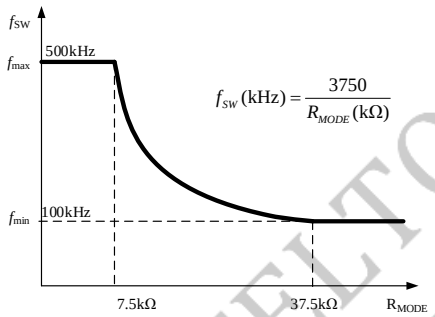


Figure 7. Switching frequency Vs. R_{MODE} in SSR mode

According to COMP voltage, JWH7232 operates in different modes for efficiency optimization. It can be divided into four operation regions. Figure 8 illustrates the frequency and peak current amplitude modulation modes. Under heavy load condition, the system operates in PWM mode, the switching is fixed at a programmed maximum frequency, Ipk will reduce from 2A to 1.6A. For medium-load range, the frequency modulation (PFM) is used to achieve high efficiency. When the load is further reduced, switching frequency is fixed at nominal 150kHz. Transitions between levels are automatically accomplished by the controller depending on the feedback voltage, V_{comp}. While working with no load or light load, the working frequency will further reduce from 150kHz to 30kHz. The minimum working frequency is set to 30kHz for noise prevention.

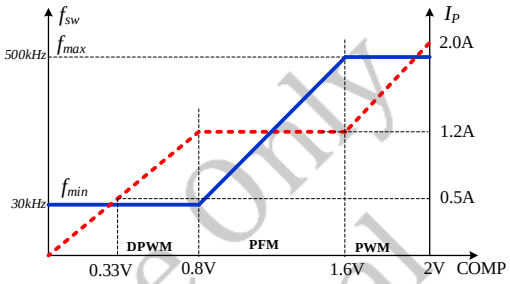


Figure 8. Switching frequency Vs. V_{COMP} in SSR mode

PSR Working Mode

JWH7232 can also be used in PSR applications as figure 9 shows.

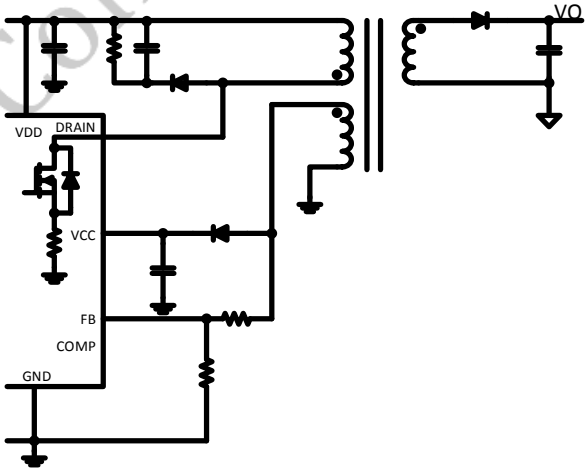


Figure 9. Typical application in PSR mode

In PSR mode, JWH7232 behaves as a multi-mode QR controller with primary-side regulation. According to the compensation voltage V_{comp}, which regulated by the output voltage, the converter operates in different modes for efficiency optimization. Figure.10

illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in figure 10.

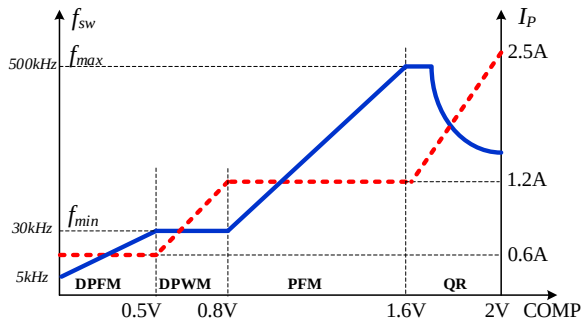


Figure 10. Switching frequency Vs. V_{COMP} in PSR mode

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to 500kHz. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is fixed to achieve high efficiency. When the load is further reduced, switching frequency is fixed at nominal 150kHz along with primary peak current varying from 48% to 24% of its maximum. While working with no load or light load, the working frequency will further reduce from 150kHz to 30kHz. The minimum working frequency is set to 30kHz for noise prevention.
In PSR mode, the compensation network is set up internally, so the COMP pin will be floating.

Output Voltage Sensing

In PSR mode, the output voltage Vo is sensed on the auxiliary winding when the magnetizing current transferred to the secondary side in PSR mode.

The waveform of a typical auxiliary winding voltage in QR mode is shown in figure 14. The accuracy of the output voltage is depended on how to get the voltage signal when inductor current reaches zero. One method is using internal dv/dt detection to detect the inflection point of Vaux during gate off. At this point, the secondary side current is approximately zero, and Vaux represents the output voltage.

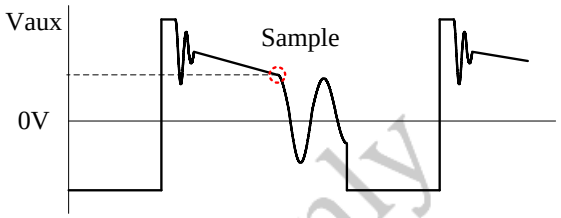


Figure 11. Typical auxiliary winding voltage Vaux waveform in QR mode.

Other Functions and Features

Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JWH7232. The frequency jittering in QR operation is achieved by peak current perturbation. The peak current is varied by ±7% around its normal value. And in other operation modes, the frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is constant 200Hz for noise prevention.

Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can't turn off the external MOSFET during the blanking time. The normal LEB time is around 150ns. Figure 12 shows the leading edge blanking time.

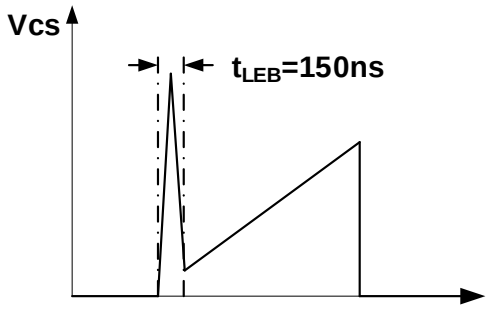


Figure 12. LEB blanking

CCM Preventing in PSR Mode

The JWH7232 working in PSR mode, when the primary-side peak current exceeds the value decided by the compensation voltage V_{comp}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after 40us to make sure the system operates in DCM.

Under light load condition, if ZCD signal has been detected before the frequency-limit signal, the switch will be turned on in 6us after the frequency-limit signal.

FB Blanking Time

In order to improve the output voltage detection accuracy and avoid the turn on spike interference, a FB blanking time is set. The FB voltage will be sensed after blanking time as figure 13 shows.

Since the transformer inductance will be greatly different with different maximum switching frequencies in SSR mode, the blanking time also needs to vary with the maximum frequency. The maximum working frequency is divided into two frequency region. When maximum working frequency is in high region (higher than 250kHz and lower than 500kHz), the maximum blanking time is 0.4us; when maximum working frequency is in low region (higher than 100kHz and lower than 250kHz), the maximum blanking time is 1.2us

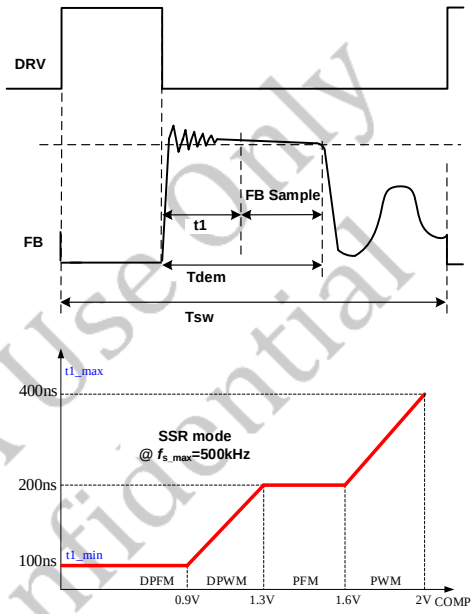


Figure 13. LEB blanking

Minimum Load Requirement

In order to sample the isolated output voltage from the primary-side flyback pulse waveform in PSR mode, the JWH7232 has to turn on and off at least for a minimum amount of time and with a minimum frequency. The JWH7232 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum energy delivery creates a minimum load requirement, which can be approximately estimated as:

$$I_{O(MIN)} = \frac{L_m \cdot I_{SW(MIN)}^{\ 2} \cdot f_{MIN}}{2V_o} \quad (3)$$

Where, L_m is the transformer primary inductance,

$I_{SW(MIN)}$ is the minimum switch current limit, f_{MIN} is the minimum switch frequency.

Slope Compensation in SSR Mode

For current mode control applications in SSR mode, the duty cycle can exceed 50%. For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. Therefore, a slope compensation is needed. Typically, D1=0.4, deltaV=1/4*V_{CS_PK}.

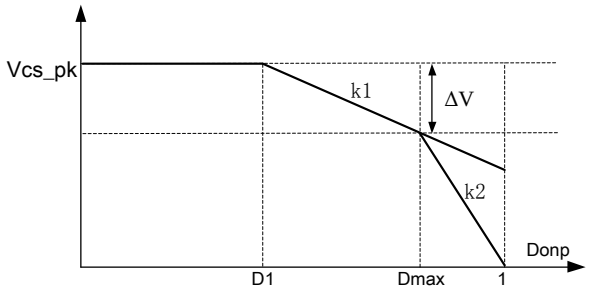


Figure 14. Slope compensation

Protection

VDD UVLO

UVLO pin is coupled to VDD pin via a resistor divider to monitor the input voltage for UVLO protection. When UVLO pin voltage V_{UVLO} is higher than a VDD UVLO threshold V_{UVLO_ON} (typically 1.2V), the controller is enabled to switching. And the controller is disabled when VDD voltage is lower than V_{UVLO_ON} for UVLO blanking time (1us typically).

During start up, if VDD voltage is below V_{UVLO_ON} when VCC reaches V_{CC_ON}, the controller will restart until VDD voltage reaches V_{UVLO_ON}. Once it occurs, VCC voltage will be pull-down quickly to restart, and the controller will start at the next time when VCC reaches V_{CC_ON} as shows.

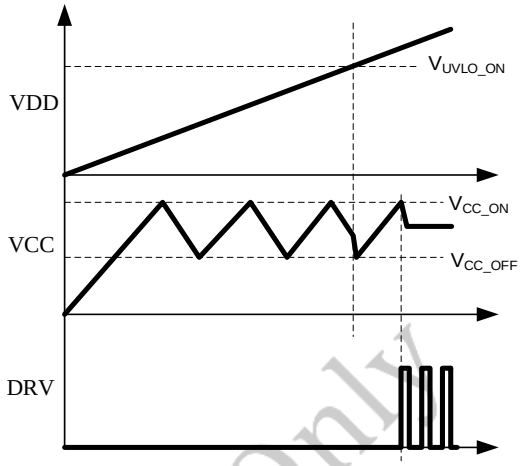


Figure 15. VDD UVLO

Primary Side SCP

The JWH7232 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the primary side current is 0.6 to 2.5A. If the primary side current exceeds the 3A SCP threshold after an internal shorter leading-edge blanking time (typical 110ns) for three consecutive cycles, the device shuts down, and then the UVLO reset and re-start fault cycle begins.

Output OVP (FB OVP)

The output over voltage protection is determined by the voltage feedback on the FB pin. If the voltage sample on FB exceeds 1.45V for three consecutive switching cycles, an FB_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins. In PSR2 mode without auxiliary winding, FB pin is coupled to SW pin through a feedback resistor R_{FB}, the output voltage can be represented by the current I_{FB} flow through R_{FB}. If I_{FB} is greater than a current threshold (typically, 120uA) for three consecutive switching cycles, an FB_OVP fault is asserted.

VCC OVP

If the voltage on VCC pin continues exceeds the Over-Voltage protection threshold (typically, 16V) more than 100us, a VCC OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

OLP

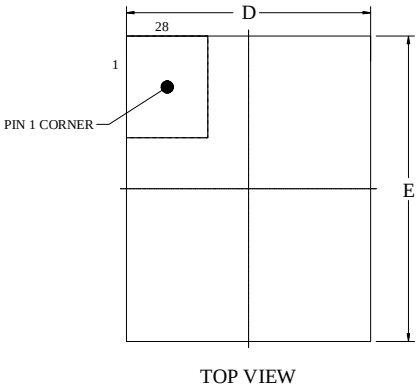
While working with heavy load, if the primary side current continues to reach the maximum current for 6ms, an OLP fault is asserted. The device shuts down, and the hiccup off time is 60ms.

Internal OTP

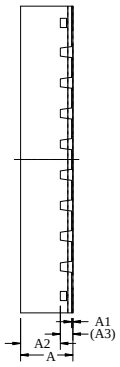
The internal over temperature protection threshold is 150°C. If the junction temperature of the device reaches this threshold, the device shuts down. When the junction temperature falls below 120°C, the device initiates the UVLO reset and re-start fault cycle.

PACKAGE OUTLINE

QFN4x5-28 Unit: mm

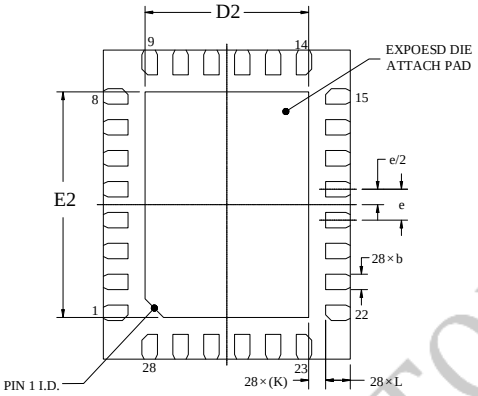


TOP VIEW



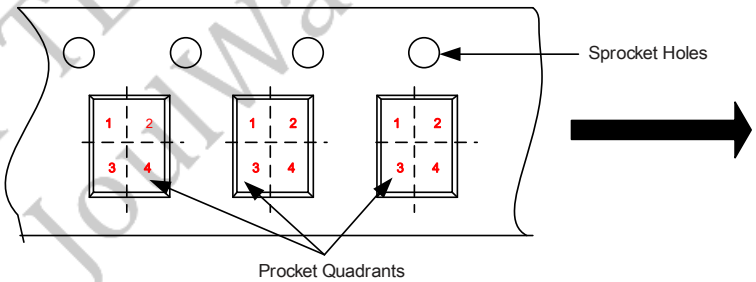
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	4.90	5.00	5.10
e		0.5 BSC	
D2	2.55	2.65	2.75
E2	3.55	3.65	3.75
L	0.3	0.4	0.5
K		0.275 REF	



BOTTOM VIEW

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	Pin1 Quadrant
QFN4x5-28	1

IMPORTANT NOTICE

- **Joulwatt Technology Inc. reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein.**
- **Any unauthorized redistribution or copy of this document for any purpose is strictly forbidden.**
- **Joulwatt Technology Inc. does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.**