DIO8018

7-Channel LDO PMIC for Camera Applications

Features

- LDO1 and LDO2:
  - input voltage: 0.6V ~ 2.0V
  - output current: 1500mA
  - output voltage: 0.504V ~ 1.504V at 8mV /step
  - dropout: 120mV at 1.2V,1500mA output
  - ±0.5% (Typ) Accuracy
- LDO3, LDO4 and LDO6
  - input voltage: 1.8V ~ 5.5V
  - output current: 300mA
  - output voltage: 1.500V~3.412V at 8mV /step
  - dropout: 100mV at 2.8V, 300mA
  - ±0.5% (Typ) Accuracy
- LDO5 and LDO7
  - input voltage: 1.8V ~ 5.5V
  - output current: 600mA
  - output voltage: 1.500V~3.412V at 8mV /step
  - dropout: 135mV at 2.8V, 600mA
  - ±0.5% (Typ) Accuracy
- Fault Interrupt
- Over temperature protection
- Programmable power up sequence
- 20-Ball WLCSP Package (1.61mm*1.96mm), 0.35mm pitch

Applications

- Smart Phone
- IP Camera
- Camera Module

Descriptions

DIO8018 is PMIC with 7 integrated LDOs, the PMIC has 2 low dropout LDOs for high current DVDD and 5 high PSRR LDOs for noise-sensitive power rails. DIO8018 has 5 independent input pins for the individual LDOs, VIN12 is for LDO1 and LDO2, VIN34 is for LDO3 and LDO4, VIN5 for LDO5, VIN6 for LDO6 and VIN7 for LDO7. DIO8018 has a separate system input VSYS which is the bias pin for the LDOs.

The LDOs' output voltage and power-up sequence can be set through the I²C interface. DIO8018 also integrated the fault monitoring features with interrupt indication.

The 7-bit I²C address of the device is 011 0101 by default but can be reprogrammed so that multiple devices can be connected to the same I²C bus.

DIO8018 is available in 1.61x1.96mm² 20 ball WLCSP package. The device is Pb-free and halogen-free.

Block Diagram

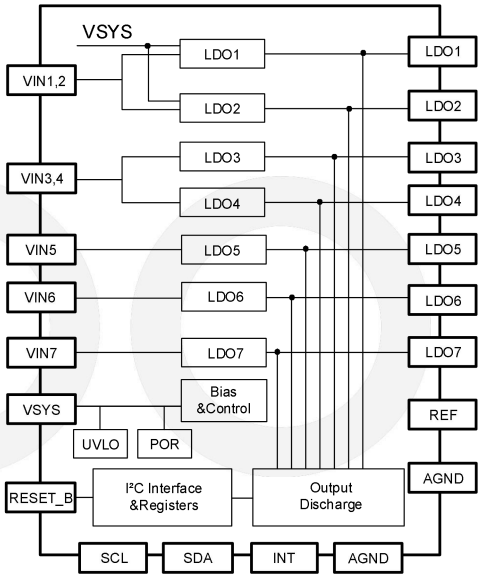


Figure 1. Application Block Diagram

Typical Applications

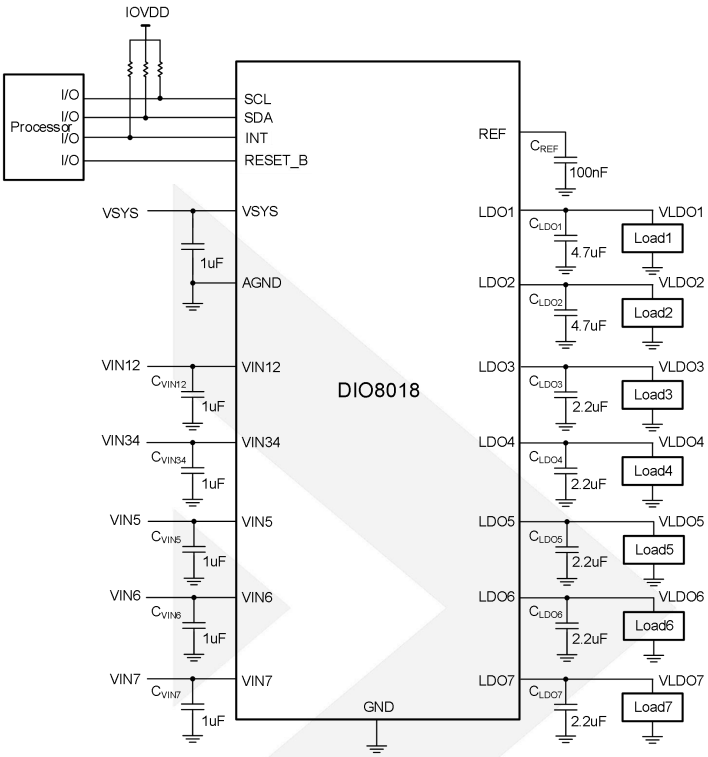


Figure 2. Typical Applications

Note:

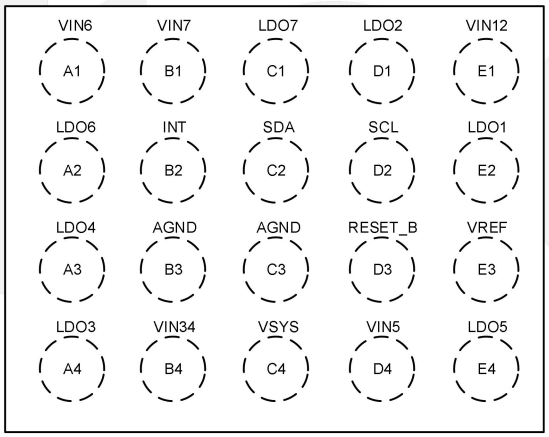
C_{LDO1-2} with minimum effective capacitance of 3.5 μF counting for capacitance changes with temperature, DC bias and package size;

C_{LDO3-7} with minimum effective capacitance of 1.5 μF counting for capacitance changes with temperature, DC bias and package size.

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO8018WL20	DV1H	Green	-40 to 85°C	WLCSP-20	Tape & Reel, 3000

Pin Assignment



WLCSP-20 (Top View)

Figure 3. Pin Configuration

Pin Descriptions

Pin	Name	Description
A1	VIN6	LDO6 input
A2	LDO6	LDO6 output
A3	LDO4	LDO4 output
A4	LDO3	LDO3 output
B1	VIN7	LDO7 input
B2	INT	The fault interrupt pin is active high indicating that an interrupt event has occurred. Open-drain output or push-pull selected by 0x12 bit<6>; the output voltage of push-pull can be selected to 1.2V or 1.8V by 0x12 bit<7>. This pin returns to low when all I^2C interrupt bits equal 0.
B3	AGND	Ground
B4	VIN3,4	LDO3 and LDO4 input
C1	LDO7	LDO7 output
C2	SDA	I^2C data line
C3	AGND	Ground
C4	VSYS	VSYS input
D1	LDO2	LDO2 output
D2	SCL	I^2C clock
D3	RESET_B	The RESET_B pin is used to enable basic circuits necessary for controlling the PMIC. The pin has an internal 100nA pull-down and should always be connected to a logic high or low.
D4	VIN5	LDO4 input
E1	VIN1,2	LDO1 and LDO2 input
E2	LDO1	LDO1 output
E3	VREF	The reference bypass pin. If used, connect a 0.1μF~0.47μF capacitor between this pin and analog ground.
E4	LDO5	LDO5 output

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
$V_{IN1,2}$	LDO1 and LDO2 input voltage	−0.5 ~3.0	V
V_{SYS}	Handset power-supply voltage	−0.5 ~ 6.5	V
$V_{IN3,4}$, V_{IN5}, V_{IN6}, V_{IN7}	LDO3, LDO4, LDO5, LDO6, LDO7 input voltage	−0.5 ~ 5.5	V
V_{CTRL}	Serial clock, serial data, Interrupt and RESET_B pin	−0.5 ~ V_{SYS} + 0.3	V
I_{PIN_MAX}	Current on Single Pin	1500	mA
T_L	Lead Temperature Range (10S)	260	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
T_J	Operating Junction Temperature Range	-40 to 150	°C
ESD	HBM	2000	V
	CDM	1500	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN12}	VIN1,2 Operating Supply Voltage Range	0.6 ~ 2.0	V
$V_{IN3,4}$, V_{IN5}, V_{IN6}, V_{IN7}	VIN3 to VIN7 Operating Supply Voltage Range	1.8 ~ V_{SYS}	V
V_{SYS}	VSYS	2.5 ~ 5.5	V
T_A	Operating Temperature Range	-40 ~ 85	°C
θ_{JA}	Thermal Resistance(1)	TBD	°C/W

DC Electrical Characteristics

Minimum and maximum values are at V_{SYS} = 2.5V or ($V_{LDO1/2}$+1.6V), which is greater; V_{IN12} = 0.6 to 2V & V_{IN12} >=$V_{LDO1/2}$ + 200mV; $V_{IN34/5/6/7}$ = 1.8 to 5.5V &$VIN_{34/5/6/7}$ >=$V_{LDO3/4/5/6/7}$ + 300mV respectively. T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = 25°C; V_{SYS}= 3.8V; V_{IN12} = 1.5V; V_{IN34} = V_{IN5} = V_{IN6} = V_{IN7} = 3.6V; $V_{LDO1/2}$ = 1.2V, $V_{LDO3/4/5/6/7}$ = 2.8V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{SYS}	Input Voltage Range		2.5		5.5	V
$V_{IN3,4}$, V_{IN5}, V_{IN6}, V_{IN7}			1.8		5.5	
$V_{IN1,2}$			0.6		2.0	
LDO1 & 2	Output Voltage Accuracy	T_A = 25°C		1.2V ±0.5		%
LDO3,4,5,6 & 7		T_A = 25°C		2.804V ±0.5		
V_{SYS_UVLO}	VSYS Under-voltage Lockout Threshold	Rising		2.35		V
		Falling		2.25		
V_{IN12_UVLO}	VIN12 Under-voltage Lockout Threshold	Rising		0.55		V
		Falling		0.45		
V_{INH_UVLO}	VIN3/4/5/6/7 Under-voltage Lockout Threshold	Rising		1.7		V
		Falling		1.6		
I_{GND}	Supply Quiescent Current	RESET_B="1", All channels are OFF		25		μA
		LDO1 is "ON"		70		
		LDO1&2 are "ON"		115		
		LDO1,2&3 are "ON"		140		
		LDO1,2,3&4 are "ON"		160		
		LDO1,2,3,4&5 are "ON"		185		
		LDO1,2,3,4,5&6 are "ON"		210		
		LDO1,2,3,4,5,6&7 are "ON"		250		
		RESET_B=5.5V, Disable IC Through I^2C		2		
I_{SD}	Supply Current Shutdown	EN = GND, V_{IN}= 3.6V		2		μA

LDO1 & 2	Output Voltage Range	When V_{OUT}+200mV<=V_{IN12}, V_{SYS}>=2.5V & V_{SYS}>=V_{OUT}+1.6V	0.504		1.504	V
LDO3 & 4	Output Voltage Range	When V_{OUT}+200mV<=V_{IN34} & V_{IN34}>=2V, V_{SYS}>=2.5V & V_{SYS}>=V_{VIN34}	1.5		3.412	V
LDO5		When V_{OUT}+200mV<=V_{IN5} & V_{IN5}>=2V, V_{SYS}>=2.5V & V_{SYS}>=V_{IN5}				
LDO6		When V_{OUT}+200mV<=V_{IN6} & V_{IN6}>=2V, V_{SYS}>=2.5V & V_{SYS}>=V_{IN6}				
LDO7		When V_{OUT}+200mV<=V_{IN7} & V_{IN7}>=2V, V_{SYS}>=2.5V				
LDO1 & 2	Dropout Voltage (2)	I_{OUT_TARGET}=1500mA, V_{OUT_TARGET} =1.2V, V_{SYS}=3.6V		120	150(3)	mV
LDO3,4,6		I_{OUT_TARGET}=300mA, V_{OUT_TARGET}=2.8V, V_{SYS}=3.6V		100		
LDO5 & 7		I_{OUT_TARGET}=600mA, V_{OUT_TARGET}=2.8V, V_{SYS}=3.6V		135		
LDO1 & 2	Max Load Current		1500			mA
LDO3,4,6			300			
LDO5,7			600			
ΔVOUT1 & 2	Line Regulation _ V_{SYS}	V_{OUT}=1.2V, I_{OUT}=1mA, V_{IN12}=1.5V, V_{SYS}=3.5V~5.5V		0.5		mV
$\Delta V_{OUT3,4,5,6\ \&\ 7}$		V_{OUT}=2.8V, I_{OUT}=1mA,V_{IN_TARGET} =3.3V, V_{SYS}=3.5V~5.5V		0.1		
$\Delta V_{OUT1\ \&\ 2}$	Line Regulation _ V_{IN}	V_{SYS}=5.5V, V_{OUT}=1.2V, I_{OUT}=1mA, V_{IN12}=1.5V~3V		0.1		mV
$\Delta V_{OUT3,4,5,6\ \&\ 7}$		V_{SYS}=5.5V, V_{OUT_TARGET} =2.8V, I_{OUT}=1mA, V_{IN_TARGET} =3.3V~5.5V		0.1		
$\Delta V_{OUT1\ \&\ 2}$	Load Regulation	I_{OUT_TARGET} =1mA ~ 1000mA		6		mV
$\Delta V_{OUT3,4,5,6\ \&\ 7}$		I_{OUT_TARGET} =1mA ~ 250mA		3		
LDO1 & 2	Output Current Limit	V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[0 or 1] = 0	1000	1300		mA
LDO1 & 2		V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[0 or 1] = 1	1500	1800		
LDO3,4,6		V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[2 or 3 or 5] = 0	350	450		
LDO3,4,6		V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[2 or 3 or 5] = 1	500	650		

LDO5,7		V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[4 or 6] = 0		500	650		
LDO5,7		V_{OUT}=90%$V_{OUT(NOM)}$, 0x02[4 or 6] = 1		700	950		
LDO1 & 2	Short Circuit Current	0x02[0 or 1] = 0		250	350		mA
LDO1 & 2		0x02[0 or 1] = 1		500	660		
LDO3,4,6		0x02[2 or 3 or 5] = 0		180	240		
LDO3,4,6		0x02[2 or 3 or 5] = 1		210	280		
LDO5,7		0x02[4 or 6] = 0		260	350		
LDO5,7		0x02[4 or 6] = 1		300	410		
LDO1 & 2	Turn-On Time	V_{OUT_TARGET} =1.2V, C_{OUT_TARGET}=4.7μF, From assertion of Enable Signal to V_{OUT} start ramp up			25		μS
LDO3,4,5,6 & 7		V_{OUT_TARGET} =2.8V, C_{OUT_TARGET} =2.2μF, From assertion of Enable Signal to V_{OUT} start ramp up			25		μS
LDO1 & 2	Soft Start Time	V_{OUT_TARGET}=1.2V, C_{OUT_TARGET} =4.7μF, V_{OUT} from 0 to 95% V_{OUT}			240		μS
LDO3,4,5,6 & 7		V_{OUT_TARGET}=2.8V, C_{OUT_TARGET} =2.2μF, V_{OUT} from 0 to 95% V_{OUT}			240		μS
LDO1 & 2	Output Noise	f=10Hz to 100kHz, I_{OUT_TARGET} =20mA			20		μVrms
LDO3,4,5,6 & 7		f=10Hz to 100kHz, I_{OUT_TARGET} =20mA			10		μVrms
$PSRR_{L1,2\_VIN}$	Power Supply Rejection Ratio on VIN1,2	LDO1 & 2 ($V_{IN1,2}$ to V_{OUT}), $V_{IN1,2}$=1.5V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_TARGET}=1.2V, I_{OUT_TARGET}=150mA, C_{IN_TARGET}=1μF, C_{OUT_TARGET} =4.7μF	f=100 Hz		85		dB
			f=1kHz		79		
			f=10 kHz		60		
			f=100 kHz		40		
			f=1MHz		40		
$PSRR_{L1,2\_VSYS}$	Power Supply Rejection Ratio on VSYS	LDO1 & 2 (V_{SYS} to V_{OUT}) $V_{IN1,2}$=1.5V, V_{SYS}=3.8V+0.2V_{PP}, V_{OUT_TARGET}=1.2V, I_{OUT_TARGET}=150mA, C_{IN_TARGET}=1μF, C_{OUT_TARGET}=4.7μF	f=100 Hz		83		dB
			f=1kHz		77		
			f=10 kHz		66		
			f=100 kHz		33		

			f=1MHz		43		
$PSRR_{L3\_VIN}$	Power Supply Rejection Ratio on VIN3	LDO3 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET}=3.6V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA, C_{IN_TARGET}=1.0μF, C_{OUT_TARGET}=2.2μF	f=100 Hz		90		dB
			f=1kHz		92		
			f=10 kHz		87		
			f=100 kHz		68		
			f=1MHz		45		
$PSRR_{L4\_VIN}$	Power Supply Rejection Ratio on VIN4	LDO4 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET}=3.6V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA, C_{IN_TARGET}=1.0μF, C_{OUT_TARGET}=2.2μF	f=100 Hz		85		dB
			f=1kHz		92		
			f=10 kHz		88		
			f=100 kHz		67		
			f=1MHz		45		
$PSRR_{L5\_VIN}$	Power Supply Rejection Ratio on VIN5	LDO5(V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET}=3.6V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA, C_{IN_TARGET}=1.0μF, C_{OUT_TARGET}=2.2μF	f=100 Hz		90		dB
			f=1kHz		90		
			f=10 kHz		85		
			f=100 kHz		73		
			f=1MHz		46		
$PSRR_{L6\_VIN}$	Power Supply Rejection Ratio on VIN6	LDO6 (V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET}=3.6V+0.2VPP, VSYS=3.8V, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA, C_{IN_TARGET}=1.0μF, C_{OUT_TARGET}=2.2μF	f=100 Hz		85		dB
			f=1kHz		87		
			f=10 kHz		83		
			f=100 kHz		65		
			f=1MHz		44		
$PSRR_{L7\_VIN}$	Power Supply Rejection Ratio on VIN7	LDO7(V_{IN_TARGET} to V_{OUT}) V_{IN_TARGET}=3.6V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA,	f=100 Hz		90		dB
			f=1kHz		85		
			f=10 kHz		82		

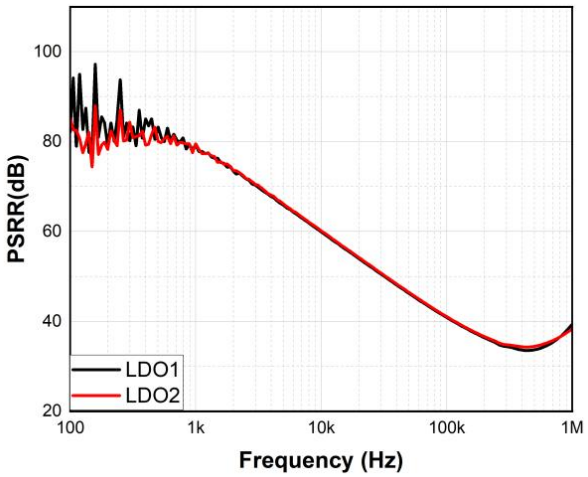
		C_{IN_TARGET}=1.0μF, C_{OUT_TARGET}=2.2μF	f=100 kHz		69		
			f=1MHz		44		
$PSRR_{L3,4,5,6,7\_VSYS}$	Power Supply Rejection Ratio on VSYS	LDO3,4,5,6,7 (V_{SYS} to V_{OUT}) $V_{IN1,2}$=1.5V, V_{IN_TARGET}=3.6, V_{SYS}=3.8V+0.2V_{PP}, V_{OUT_TARGET}=2.8V, I_{OUT_TARGET}=100mA, C_{IN_TARGET}=1.0μF, C_{OUT_TARGET} =2.2μF	f=100 Hz		85		dB
			f=1kHz		92		
			f=10 kHz		79		
			f=100 kHz		56		
			f=1MHz		45		
T_{WRN}	Thermal Warning				115		°C
T_{SD}	Thermal Shutdown				150		°C
T_{HYS}	Thermal Hysteresis for T_{SD} and T_{WRN}				25		°C
LDO1 & 2	Active Output Discharge Resistance				100		Ω
LDO3,4,5,6 & 7					100		
LDO1 & 2	Line Transient	V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10μs, I_{OUT} = 1 mA		-1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30μs, I_{OUT} = 1 mA				1	
LDO3,4,5,6 & 7		V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10μs, I_{OUT} = 1 mA		-1			
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30μs, I_{OUT} = 1 mA				1	
LDO1 & 2	Load Transient	I_{OUT_TARGET} =1mA to 500mA in 5μs			-30		mV
		I_{OUT_TARGET} =500mA to 1mA in 5μs			30		
LDO3,4,5,6 & 7		I_{OUT_TARGET} =1mA to 300mA in 5μs			-20		
		I_{OUT_TARGET} =300mA to 1mA in 5μs			20		
RESET_B Logic Inputs							
I_{LEAK}	Input Leakage				0.1	0.5	μA
V_{IH}	Input HIGH Voltage			0.8			V
V_{IL}	Input LOW Voltage					0.4	V
INT Logic Output							
I_{LEAK}	Input Leakage				0.1	0.2	μA
V_{OH}	Output HIGH Voltage	I_{OUT}=10mA		1.0	1.2		V

V_{OL}	Input LOW Voltage	I_{SINK}=10mA			0.3	V
I²C Logic						
I_{LEAK}	Input Leakage			0.1	0.2	μA
V_{IH}	Input HIGH Voltage		1.2			V
V_{IL}	Input LOW Voltage				0.4	V
I_{OL}	SDA Sink Current		20			mA
F_{SCL}	SCL Clock Frequency		100	400	1000	kHz
t_{BUF}	Bus−Free Time Between STOP and START Conditions		0.5			us
$t_{HD;STA}$	START or Repeated START Hold Time		260			ns
t_{LOW}	SCL LOW Period		0.5			ns
t_{HIGH}	SCL HIGH Period		260			ns
$t_{SU;STA}$	Repeated START Setup Time		260			ns
$t_{SU;DAT}$	Data Setup Time		50			ns
$t_{VD;DAT}$	Data Valid Time				450	ns
$t_{VD;ACK}$	Data Valid Acknowledge Time				450	ns
t_R	SDA and SCL Rise Time				120	ns
t_F	SDA and SCL Fall Time		6.55		120	ns
$t_{SU;STO}$	Stop Condition Setup Time		260			ns
Ci	SDA and SCL Input Capacitance		10			pF
Cb	Capacitive Load for SDA and SCL		550			pF
t_{SP}	Spike pulse width that input filter must be suppress		0		50	ns

Note:2.Only by Design Guaranteed Spec.

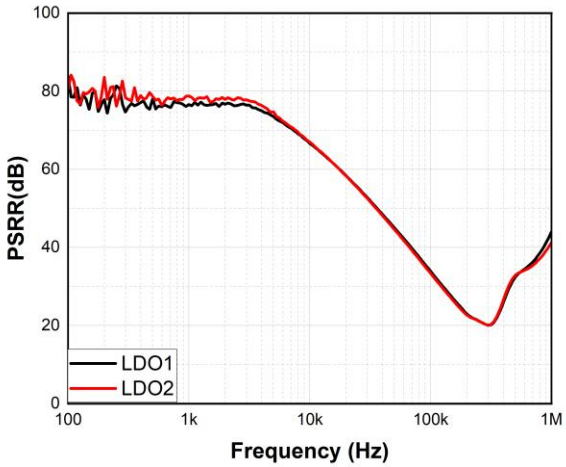
Note:3.Max. Dropout value 150mV in 25°C, Max. Dropout value 200mV value in 125°C.

Typical Performance Characteristics



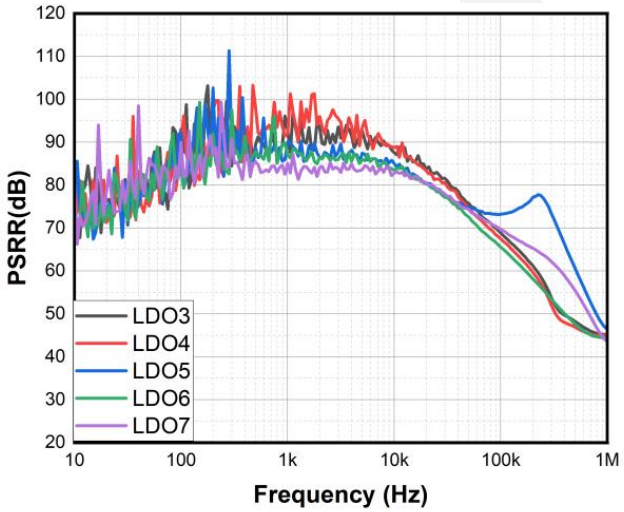
$V_{IN1,2}$ to V_{OUT}, $V_{IN1,2}$ = 1.5V + 0.2V_{PP}, V_{OUT}=1.2V, I_L=150mA, C_{OUT}=4.7uF

Figure 4. PSRR vs Frequency



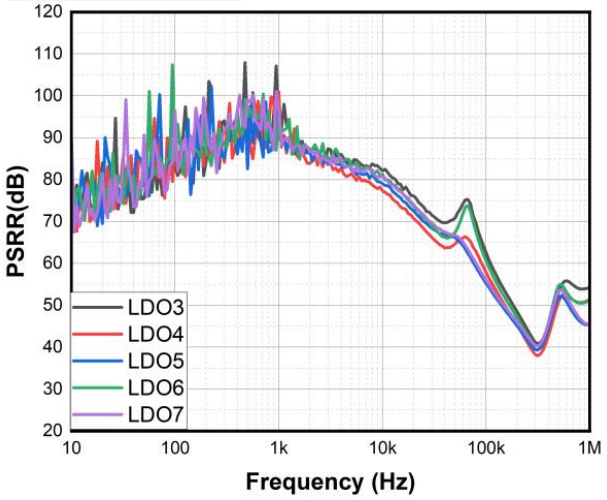
V_{SYS} to $V_{OUT1,2}$, V_{SYS}=3.8V+0.2V_{PP}, V_{OUT12}=1.2V, I_L=150mA, C_{OUT}=4.7uF

Figure 5. PSRR vs Frequency



$V_{IN3,4,5,6,7}$ to V_{OUT}, $V_{IN3,4,5,6,7}$=3.6V + 0.2V_{PP}, V_{OUT}=2.8V, I_L=100mA, C_{OUT}=2.2uF

Figure 6. PSRR vs Frequency



V_{SYS} to $V_{OUT3,4,5,6,7}$, V_{SYS}=3.8V+0.2V_{PP}, $V_{OUT3,4,5,6,7}$=2.8V, I_L=100mA, C_{OUT}=2.2uF

Figure 7. PSRR vs Frequency

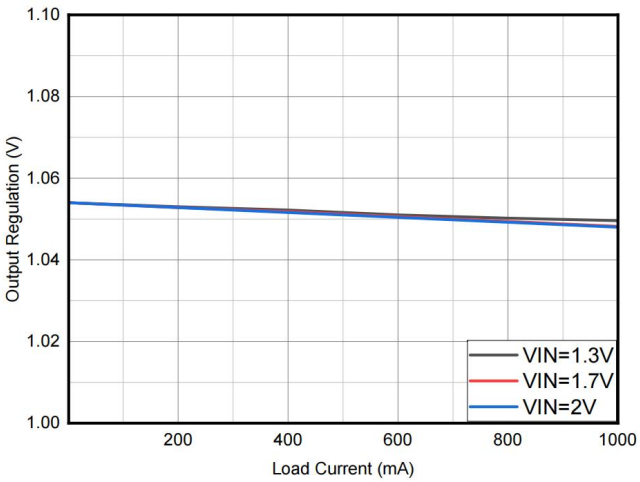


Figure 8. LDO1/2 Output Regulation vs. Load Current input Voltage, V_{OUT}=1.05V

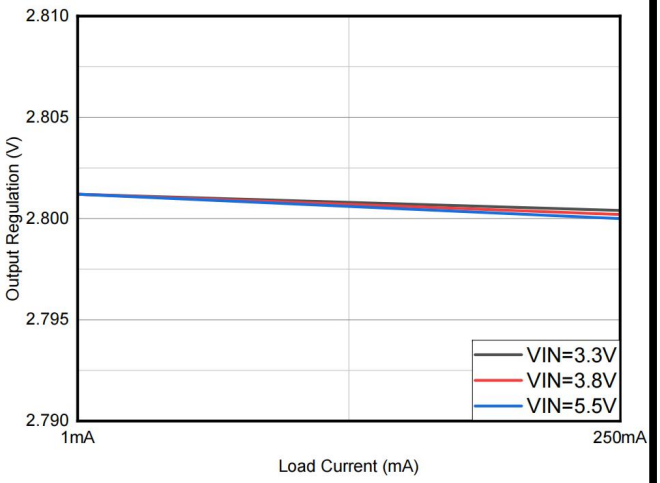


Figure 9. LDO3/4/6 Output Regulation vs. Load Current Input Voltage, V_{OUT}=2.8V

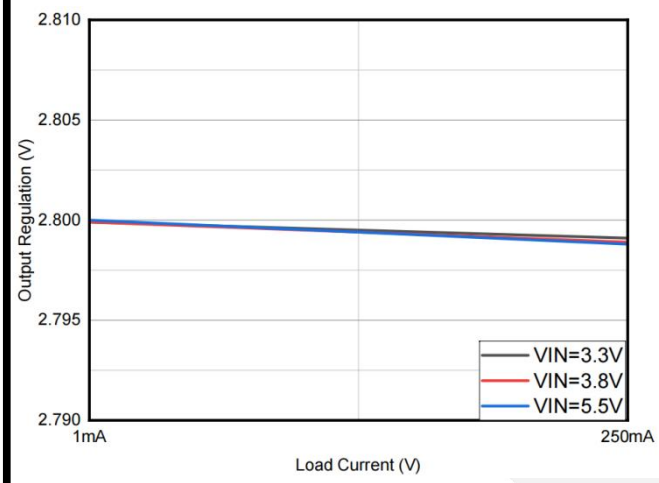


Figure 10. LDO5/7 Output Regulation vs. Load Current Input Voltage, V_{OUT}=2.8V

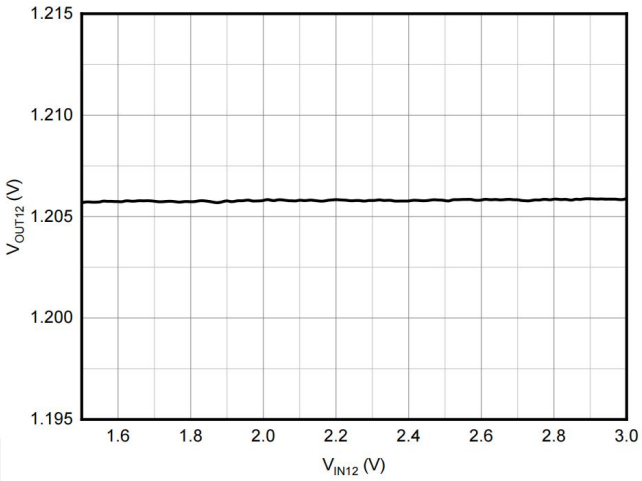


Figure 11. LDO1/2 Output Regulation vs. Input Voltage

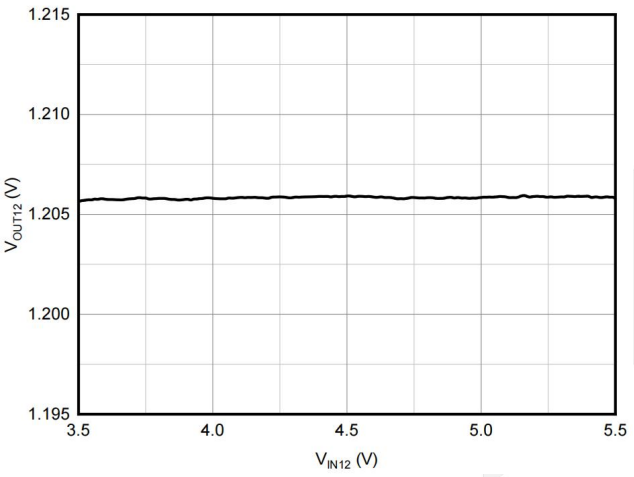


Figure 12. LDO1/2 Output Regulation vs. System Input Voltage

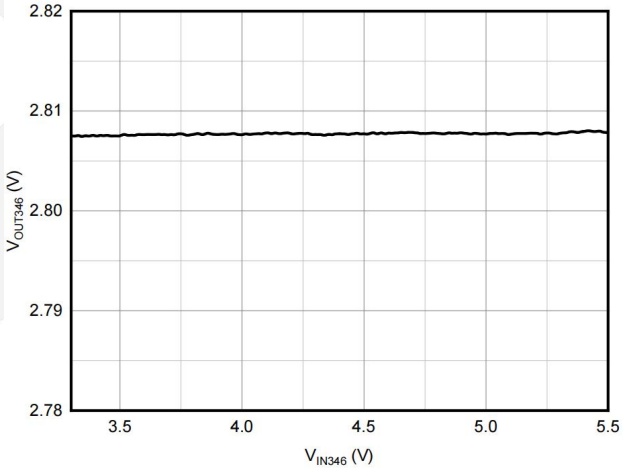


Figure 13. LDO3/4/6 Output Regulation vs. Input Voltage

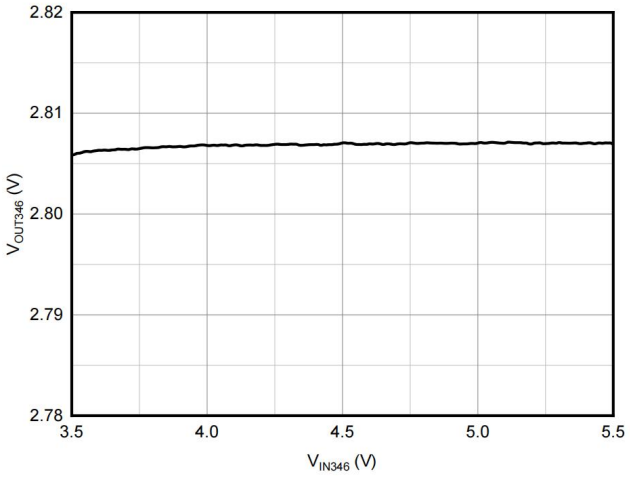


Figure 14. LDO3/4/6 Output Regulation vs. System Input Voltage

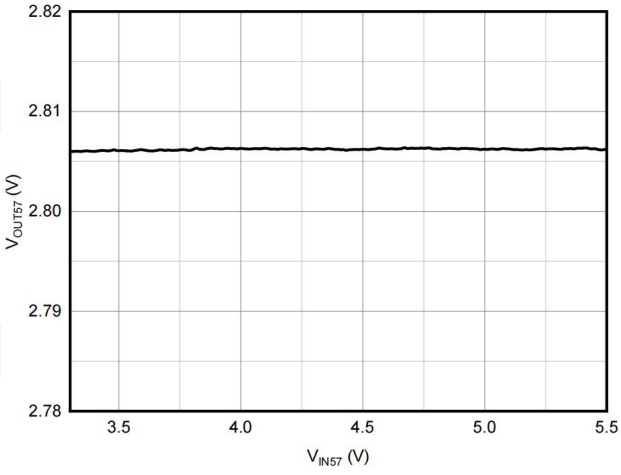


Figure 15. LDO5/7 Output Regulation vs. Input Voltage

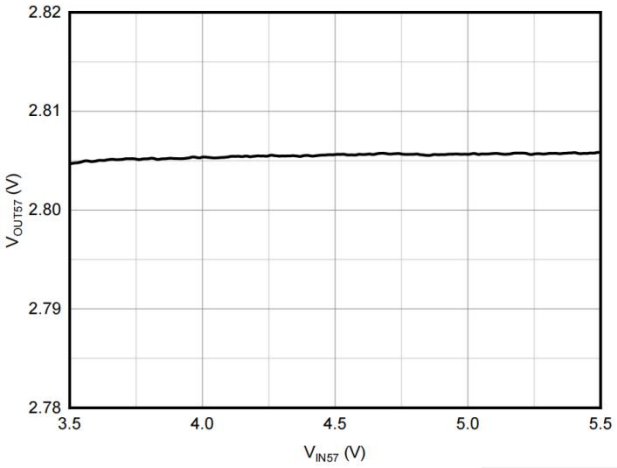


Figure 16. LDO5/7 Output Regulation vs. System Input Voltage

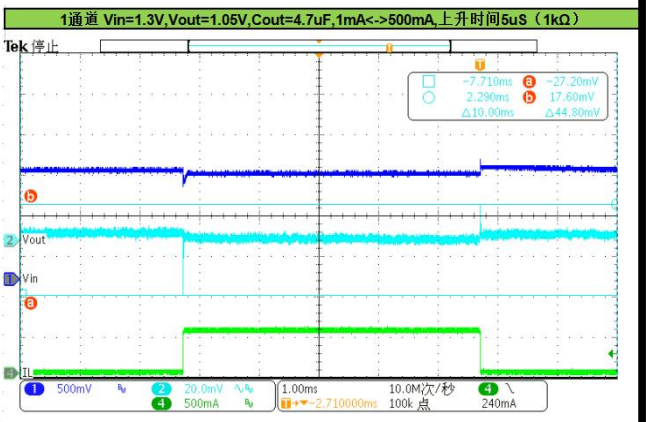


Figure 17. LDO1/2 Load Transient

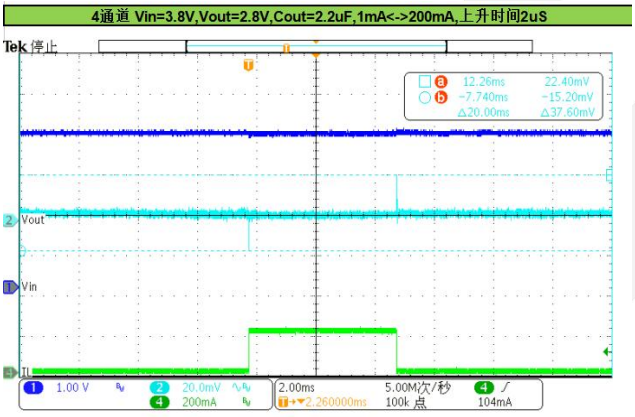


Figure 18. LDO3/4/6 Load Transient

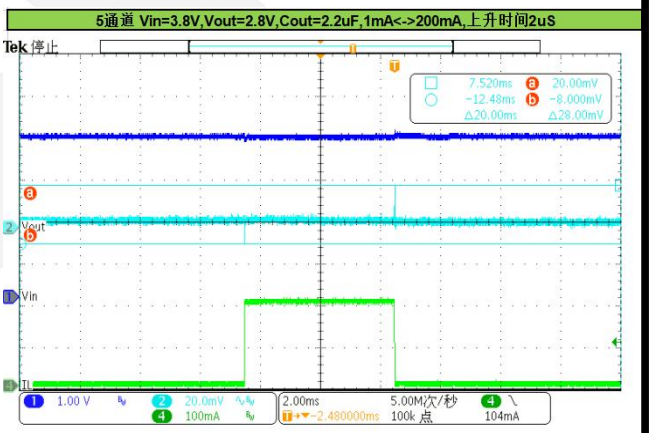


Figure 19. LDO5/7 Load Transient

Detailed Description

Overview

The DIO8018 micro Power Management IC(PMIC) is optimized to supply power to different sub-systems of battery-powered mobile applications. It integrates seven low−dropout regulators: two high current LDOs, three ultra low noise / high PSRR LDOs, and two LDOs for general purpose. The features of the DIO8018 can be programmed through an I^2C interface.

Under Voltage Lockout (UVLO)

When the RESET_B pin is pulled high, if VSYS is above Power−On Reset (POR) voltage but below its UVLO rising threshold, or if VINs of the LDOs are below their UVLO rising threshold, the assigned UVLO interrupt bit and UVLO status bit will be set, and the INT pin will be asserted high. The UVLO status bit remains set as long as the input voltage is below its UVLO rising threshold.

When VSYS or VINs fall below their UVLO falling threshold, the LDO(s) will shut down, and an UVLO interrupt will be declared. The UVLO status bit remains set until the input voltage rises above its UVLO rising threshold, and the LDO(s) performs startup immediately.

The suspend bits will be set upon shutdown. The LDO(s) will stay in shutdown for a minimum of 20ms and then attempt a restart if VSYS or VINs have risen above their UVLO rising threshold. The suspend bits are cleared upon restart. The LDO(s) will be disabled permanently after the 4th UVLO fault.

Thermal Management

When the die temperature rises to a nominal 115°C, the Thermal Warning status bit will be set to “1” and remain set until the die temperature drops to a nominal 100°C.

If the die temperature continues to rise to a nominal 155°C, a Thermal Shutdown event is activated, all the LDOs are disabled, and the Thermal Shutdown interrupt bit is set but I^2C communication remains. The Thermal Shutdown status bit is also set and will remain set as long as the device is above the Thermal Warning temperature. The chip suspend bit is set upon shutdown.

After the die temperature falls below the Thermal Warning threshold, the Thermal Shutdown status and chip suspend bits will be cleared, and the device will return to the operating conditions prior to the thermal shutdown event.

Enabling / Disabling

The DIO8018 LDOs can be enabled and disabled independently with the LDOx_EN bits in the ENABLE register. To enable DIO8018 LDOs, with RESET_B pin high, set the LDOx_EN bits to “1”. The DIO8018 LDOs have an internal soft−start, which limits the inrush current to the ILIM setting. The LDOs will ignore faults during the first 1.5ms at startup. After 1.5ms, if the LDO output fails to reach the UVP rising threshold, a UVP fault will be declared.

To disable the DIO8018 LDOs, set the LDOx_EN bits to “0”. The active discharge feature is enabled by default, with which, a 100Ω resistor is connected between VOUT and GND to discharge the output capacitors when the LDOx_en bits are set to “0”.

To do a global shutdown of all LDOs, set the RESET_B pin low.

Over−current Protection (OCP)

The LDOs are protected from excessive load and short−circuit. The current limit level can be programmed through the I^2C interface.

When an over−load event occurs, the current is automatically limited to the programmed current limit. And once the current limit is detected, the associated OCP status bit is set, and if the LDO remains in current limit for more than 1ms, the OCP interrupt bit will be set and the INT pin will be pulled high. Then the LDO will shut down permanently without attempting any restart; meanwhile, the associated suspend bit is set and the status bit is cleared.

The OCP debounce timer is programmable through I^2C.

Under Voltage Protection (UVP)

If the output voltage falls approximately 20% (10% for LDO1/2) below the target VOUT and the fault persists for more than 100μs, the associated UVP status bit and the UVP interrupt bit will be set. The INT pin will be pulled high at the same time. The LDO will then be disabled, the associated status bit is cleared and the suspend bit is set. The interrupt bit will be cleared upon a read of the bit.

4−Fault Shutdown

To prevent repetitive starting and faulting of an LDO or of the IC itself, detection of 4 failures will result in a permanent shutdown of the LDO, or if it is a system fault, the entire IC will shut down permanently.

Individual LDO Fault: the LDO will be latched−off after the 4th individual LDO fault (any combination of UVP, and/or OCP, and/or VINx UVLO), and the LDOx_EN bit will be cleared. In order to clear the latch−off and re−enable the LDOs, set the LDOx_EN bits to “1”.

Chip Fault: all the LDOs will be latched−off after the 4th chip fault (any combination of Thermal Shutdown, and/or VSYS UVLO) with all the LDOx_EN bits cleared. In order to clear the latch−off, the RESET_B pin needs to be pulled low.

Reset

When the RESET_B pin is pulled low, any interrupt bits and status bits will be cleared. Additionally, all fault counters will reset to 0. However, all the other registers will remain set to the previous values.

In order to reset all the I^2C registers to their default values, write a “1011” to bit [7:4] in the RESET register.

Power Up/Down Sequence

Power-up and power-down sequences can be programmed and controlled with the dedicated registers xxxx_SEQ and SEQUENCING.

If an LDO faults during a start−up sequence, the other LDOs will still be starting up in their assigned time slot. The xxxx_SEQ register bits for the faulted LDO will remain set to the previous values. The system can then attempt to start the faulted LDO in another sequence by setting the SEQ_CONTROL bits to “01” or by clearing the xxxx_SEQ bits to “000” and writing a “1” to the enable bit for the faulted LDO.

No Fault Shutdown

DIO8018 provides a “No Fault Shutdown” feature, which prevents LDOs from shutting down during an OCP or UVP event. It is activated by setting the FLT_SD_B bit in the RESET register to “1”.

By setting FLT_SD_B to “1”, it prevents the shutdown during an OCP or UVP event, but not during an LDO VIN UVLO event. With FLT_SD_B=1, when LDO VIN UVLO, OCP event occurs, the interrupt and status bits will still indicate the fault has occurred, but the fault counter will not be incremented.

I2C Functionality

I^2C Interface

The DIO8018 serial interface is compatible with Standard, Fast and Fast Plus Mode I^2C Bus specifications. The

SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

The default I²C slave address is shown in Table 3. The LSB of the address byte is used as the read/write bit and is not included in the 7-bit Hex, Decimal, or Binary value as shown in Table 1. Table 2 is provided to show the location of the R/W bit.

The I²C address can also be changed by setting it in the I²C_ADDR_SEL register.

Device	Hex	Decimal	7 bit Binary
DIO8018	35h	53d	011 0101

Table 1. I²C SLAVE ADDRESS

7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	R/W

Table 2. I²C (7 bit) SLAVE ADDRESS BYTE

Bus Timing

As shown in Figure 20, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

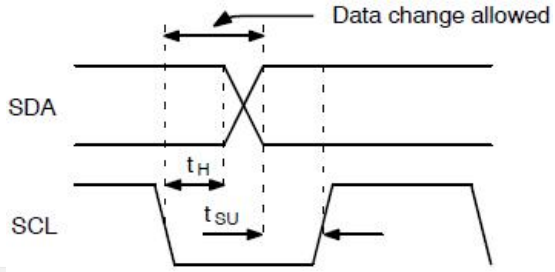


Figure 20. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 21.

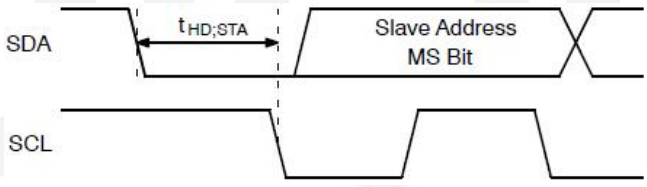


Figure 21. Data Transfer on I²C Serial Bus

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 22.

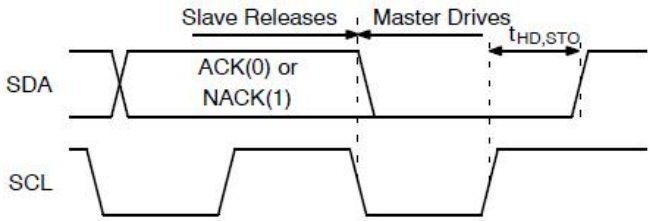


Figure 22. Stop Bit

During a read from the DIO8018, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH, as shown in Figure 23.

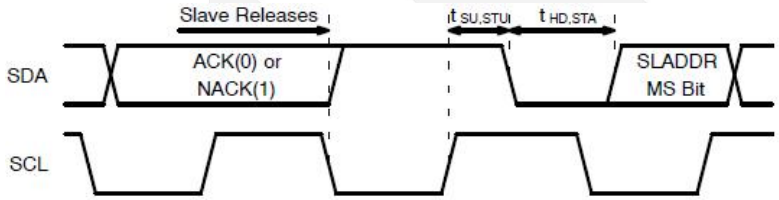


Figure 23. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as “Master Drives Bus” and “Slave Drives Bus”. All addresses and data are MSB first.

Multi−Byte (Sequential) Read and Write Transactions

Sequential Write (Figure 26)

The Slave Address, Reg Addr address, and the first data byte are transmitted to the DIO8018 in the same way as in a single−byte write (Figure 24). However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte is written and its ACK bit is received, the master issues a STOP bit. The IC contains an 8−bit counter that increments the address pointer after each byte is written.

Sequential Read (Figure 27)

Sequential reads are initiated in the same way as a single−byte read (Figure 25), except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave’s I^2C logic to transmit the next sequentially addressed 8−bit word. The DIO8018 contains an 8−bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one I^2C transaction.

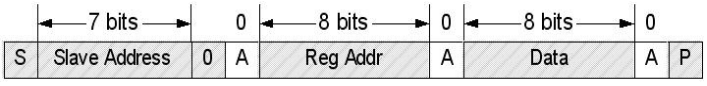


Figure 24. Single−Byte Write Transaction

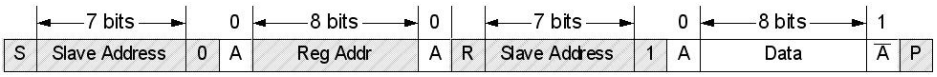


Figure 25. Single−Byte Read Transaction

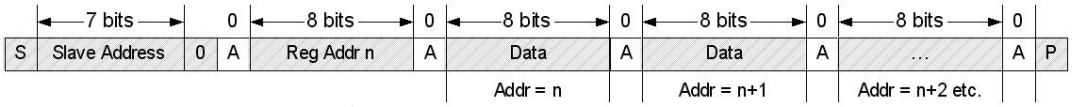


Figure 26. Multi−Byte (Sequential) Write Transaction

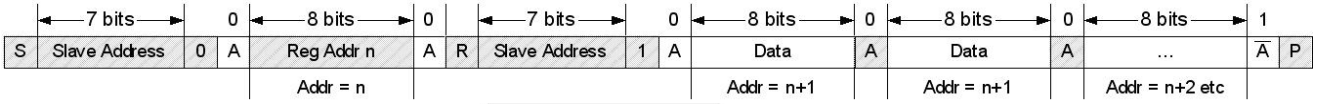


Figure 27. Multi−Byte (Sequential) Read Transaction

Register Maps

ADDR	Register Name	Type	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	PRODUCT ID	R	04	Device ID							
0x01	SILICON REV ID	R	01	Revision							
0x02	IOUT	R/W	53	0	LDO7_ILIM	LDO6_ILIM	LDO5_ILIM	LDO4_ILIM	LDO3_ILIM	LDO2_ILIM	LDO1_ILIM
0x03	ENABLE	R/W	80	VSYS_EN	LDO7_EN	LDO6_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN
0x04	LDO1	R/W	95	LDO1_VOUT							
0x05	LDO2	R/W	95	LDO2_VOUT							
0x06	LDO3	R/W	B3	LDO3_VOUT							
0x07	LDO4	R/W	B3	LDO4_VOUT							
0x08	LDO5	R/W	B3	LDO5_VOUT							
0x09	LDO6	R/W	B3	LDO6_VOUT							
0x0A	LDO7	R/W	B3	LDO7_VOUT							
0x0B	LDO12_SEQ	R/W	00	0		LDO2_SEQ			LDO1_SEQ		
0x0C	LDO34_SEQ	R/W	00	0		LDO4_SEQ			LDO3_SEQ		
0x0D	LDO56_SEQ	R/W	00	0		LDO6_SEQ			LDO5_SEQ		
0x0E	LDO7_SEQ	R/W	00	0					LDO7_SEQ		
0x0F	SEQUENCING	R/W	00	SEQ_SPEED		SEQ_CONTROL		SEQ_ON	SEQ_COUNT		
0x10	DISCHARGE	R/W	7F	0	LDO1_DIS	LDO2_DIS	LDO3_DIS	LDO4_DIS	LDO5_DIS	LDO6_DIS	LDO7_DIS
0x11	RESET	R/W	06	SOFT_RESET				0	OCP_TIMER		FLT_SD_B

0x12	I²C_ADDR	R/W	81	INT_LEVEL_SEL	INT_OutMode_SEL	0				I²C_ADDR_SEL	
0x13	RESERVED	R/W	00	0	0	0	0	0	0	0	0
0x14	RESERVED	R/W	00	0	0	0	0	0	0	0	0
0x15	INTERRUPT1	R/C	00	0	LDO7_UVP_INT	LDO6_UVP_INT	LDO5_UVP_INT	LDO4_UVP_INT	LDO3_UVP_INT	LDO2_UVP_INT	LDO1_UVP_INT
0x16	INTERRUPT2	R/C	00	0	LDO7_OCP_INT	LDO6_OCP_INT	LDO5_OCP_INT	LDO4_OCP_INT	LDO3_OCP_INT	LDO2_OCP_INT	LDO1_OCP_INT
0x17	INTERRUPT3	R/C	00	TSD_INT	TSD_WRN_INT	VSYS_UVLO_INT	LDO7_UVLO_INT	LDO6_UVLO_INT	LDO5_UVLO_INT	LDO34_UVLO_INT	LDO12_UVLO_INT
0x18	STATUS1	R	00	0	LDO7_UVP_STAT	LDO6_UVP_STAT	LDO5_UVP_STAT	LDO4_UVP_STAT	LDO3_UVP_STAT	LDO2_UVP_STAT	LDO1_UVP_STAT
0x19	STATUS2	R	00	0	LDO7_OCP_STAT	LDO6_OCP_STAT	LDO5_OCP_STAT	LDO4_OCP_STAT	LDO3_OCP_STAT	LDO2_OCP_STAT	LDO1_OCP_STAT
0x1A	STATUS3	R	00	TSD_STAT	TSD_WRN_STAT	VSYS_UVLO_STAT	LDO7_UVLO_STAT	LDO6_UVLO_STAT	LDO5_UVLO_STAT	LDO34_UVLO_STAT	LDO12_UVLO_STAT
0x1B	STATUS4	R	00	CHIP_SUSD	LDO7_SUSD	LDO6_SUSD	LDO5_SUSD	LDO4_SUSD	LDO3_SUSD	LDO2_SUSD	LDO1_SUSD
0x1C	MINT1	R/W	00	0	MASK_LDO7_UVP	MASK_LDO6_UVP	MASK_LDO5_UVP	MASK_LDO4_UVP	MASK_LDO3_UVP	MASK_LDO2_UVP	MASK_LDO1_UVP
0x1D	MINT2	R/W	00	0	MASK_LDO7_OCP	MASK_LDO6_OCP	MASK_LDO5_OCP	MASK_LDO4_OCP	MASK_LDO3_OCP	MASK_LDO2_OCP	MASK_LDO1_OCP
0x1E	MINT3	R/W	00	MASK_TSD	MASK_TSD_WRN	MASK_VSYS_UVLO	MASK_LDO7_UVLO	MASK_LDO6_UVLO	MASK_LDO5_UVLO	MASK_LDO34_UVLO	MASK_LDO12_UVLO

REGISTER DETAILS – 0x00 PRODUCT ID

Default = 00000100

Bits	Name	Default	Type	Description	
7:0	Product ID	0000 0100	Read	Identifies vendor and device type	
				Code	**Product**
				00000100	DIO8018

REGISTER DETAILS – 0x01 SILICON REV ID

Default = 00000001

Bits	Name	Default	Type	Description
7:0	Revision	0000 0001	Read	Identifies silicon revision

REGISTER DETAILS – 0x02 IOUT

Default = 01010011

Bits	Name	Default	Type	Description	
7	UNUSED	0	R/W		
6	LDO7_ILIM	1	R/W	**Code**	**Current Limit**
				0	650 mA
				1	950 mA
5	LDO6_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
4	LDO5_ILIM	1	R/W	**Code**	**Current Limit**
				0	650 mA
				1	950 mA
3	LDO4_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
2	LDO3_ILIM	0	R/W	**Code**	**Current Limit**
				0	450 mA
				1	650 mA
1	LDO2_ILIM	1	R/W	**Code**	**Current Limit**
				0	1300 mA
				1	1800 mA
0	LDO1_ILIM	1	R/W	**Code**	**Current Limit**
				0	1300 mA
				1	1800 mA

REGISTER DETAILS – 0x03 ENABLE

Default = 10000000

Bits	Name	Default	Type	Description
7	VSYS_EN	1	R/W	Enable bit for System. The system bias will be getting ready for enabling individual LDO if bit7=1 and RESET_N is pulled high
				Code / **Status of SYS**
				0 / Disabled
				1 / Enabled
6	LDO7_EN	0	R/W	Enable bit for LDO7. This bit only controls the state of LDO7 if LDO7_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
5	LDO6_EN	0	R/W	Enable bit for LDO6. This bit only controls the state of LDO6 if LDO6_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
4	LDO5_EN	0	R/W	Enable bit for LDO5. This bit only controls the state of LDO5 if LDO5_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
3	LDO4_EN	0	R/W	Enable bit for LDO4. This bit only controls the state of LDO4 if LDO4_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
2	LDO3_EN	0	R/W	Enable bit for LDO3. This bit only controls the state of LDO3 if LDO3_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
1	LDO2_EN	0	R/W	Enable bit for LDO2. This bit only controls the state of LDO2 if LDO2_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled
0	LDO1_EN	0	R/W	Enable bit for LDO1. This bit only controls the state of LDO1 if LDO1_SEQ = 000.
				Code / **Status of LDO**
				0 / Disabled
				1 / Enabled

REGISTER DETAILS – 0x04 LDO1

Default = 10010101

Bits	Name	Size	Type	Description
7:0	LDO1_ VOUT	0000 0000	R/W	Sets LDO1 regulation target voltage. Equation: V_{OUT} = 0.800 V + [(d − 99) x 8 mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
00	Reserved	40	0.520V	80	1.032V	C0	Reserved
01	Reserved	41	0.528V	81	1.040V	C1	Reserved
02	Reserved	42	0.536V	82	1.048V	C2	Reserved
03	Reserved	43	0.544V	83	1.056V	C3	Reserved
04	Reserved	44	0.552V	84	1.064V	C4	Reserved
05	Reserved	45	0.560V	85	1.072V	C5	Reserved
06	Reserved	46	0.568V	86	1.080V	C6	Reserved
07	Reserved	47	0.576V	87	1.088V	C7	Reserved
08	Reserved	48	0.584V	88	1.096V	C8	Reserved
09	Reserved	49	0.592V	89	1.104V	C9	Reserved
0A	Reserved	4A	0.600V	8A	1.112V	CA	Reserved
0B	Reserved	4B	0.608V	8B	1.120V	CB	Reserved
0C	Reserved	4C	0.616V	8C	1.128V	CC	Reserved
0D	Reserved	4D	0.624V	8D	1.136V	CD	Reserved
0E	Reserved	4E	0.632V	8E	1.144V	CE	Reserved
0F	Reserved	4F	0.640V	8F	1.152V	CF	Reserved
10	Reserved	50	0.648V	90	1.160V	D0	Reserved
11	Reserved	51	0.656V	91	1.168V	D1	Reserved
12	Reserved	52	0.664V	92	1.176V	D2	Reserved
13	Reserved	53	0.672V	93	1.184V	D3	Reserved
14	Reserved	54	0.680V	94	1.192V	D4	Reserved
15	Reserved	55	0.688V	**95**	**1.200V**	D5	Reserved
16	Reserved	56	0.696V	96	1.208V	D6	Reserved
17	Reserved	57	0.704V	97	1.216V	D7	Reserved
18	Reserved	58	0.712V	98	1.224V	D8	Reserved
19	Reserved	59	0.720V	99	1.232V	D9	Reserved
1A	Reserved	5A	0.728V	9A	1.240V	DA	Reserved
1B	Reserved	5B	0.736V	9B	1.248V	DB	Reserved
1C	Reserved	5C	0.744V	9C	1.256V	DC	Reserved
1D	Reserved	5D	0.752V	9D	1.264V	DD	Reserved

7:0	LDO1_ VOUT	0000 0000	R/W	1E	Reserved	5E	0.760V	9E	1.272V	DE	Reserved
				1F	Reserved	5F	0.768V	9F	1.280V	DF	Reserved
				20	Reserved	60	0.776V	A0	1.288V	E0	Reserved
				21	Reserved	61	0.784V	A1	1.296V	E1	Reserved
				22	Reserved	62	0.792V	A2	1.304V	E2	Reserved
				23	Reserved	63	0.800V	A3	1.312V	E3	Reserved
				24	Reserved	64	0.808V	A4	1.320V	E4	Reserved
				25	Reserved	65	0.816V	A5	1.328V	E5	Reserved
				26	Reserved	66	0.824V	A6	1.336V	E6	Reserved
				27	Reserved	67	0.832V	A7	1.344V	E7	Reserved
				28	Reserved	68	0.840V	A8	1.352V	E8	Reserved
				29	Reserved	69	0.848V	A9	1.360V	E9	Reserved
				2A	Reserved	6A	0.856V	AA	1.368V	EA	Reserved
				2B	Reserved	6B	0.864V	AB	1.376V	EB	Reserved
				2C	Reserved	6C	0.872V	AC	1.384V	EC	Reserved
				2D	Reserved	6D	0.880V	AD	1.392V	ED	Reserved
				2E	Reserved	6E	0.888V	AE	1.400V	EE	Reserved
				2F	Reserved	6F	0.896V	AF	1.408V	EF	Reserved
				30	Reserved	70	0.904V	B0	1.416V	F0	Reserved
				31	Reserved	71	0.912V	B1	1.424V	F1	Reserved
				32	Reserved	72	0.920V	B2	1.432V	F2	Reserved
				33	Reserved	73	0.928V	B3	1.440V	F3	Reserved
				34	Reserved	74	0.936V	B4	1.448V	F4	Reserved
				35	Reserved	75	0.944V	B5	1.456V	F5	Reserved
				36	Reserved	76	0.952V	B6	1.464V	F6	Reserved
				37	Reserved	77	0.960V	B7	1.472V	F7	Reserved
				38	Reserved	78	0.968V	B8	1.480V	F8	Reserved
				39	Reserved	79	0.976V	B9	1.488V	F9	Reserved
				3A	Reserved	7A	0.984V	BA	1.496V	FA	Reserved
				3B	Reserved	7B	0.992V	BB	1.504V	FB	Reserved
				3C	Reserved	7C	1.000V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008V	BD	Reserved	FD	Reserved
				3E	0.504V	7E	1.016V	BE	Reserved	FE	Reserved
				3F	0.512V	7F	1.024V	BF	Reserved	FF	Reserved

REGISTER DETAILS – 0x05 LDO2

Default = 10010101

Bits	Name	Default	Type	Description
7:0	LDO2_ VOUT	0000 0000	R/W	Sets LDO2 regulation target voltage. Equation: V_{OUT} = 0.800V + [(d − 99) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
00	Reserved	40	0.520V	80	1.032V	C0	Reserved
01	Reserved	41	0.528V	81	1.040V	C1	Reserved
02	Reserved	42	0.536V	82	1.048V	C2	Reserved
03	Reserved	43	0.544V	83	1.056V	C3	Reserved
04	Reserved	44	0.552V	84	1.064V	C4	Reserved
05	Reserved	45	0.560V	85	1.072V	C5	Reserved
06	Reserved	46	0.568V	86	1.080V	C6	Reserved
07	Reserved	47	0.576V	87	1.088V	C7	Reserved
08	Reserved	48	0.584V	88	1.096V	C8	Reserved
09	Reserved	49	0.592V	89	1.104V	C9	Reserved
0A	Reserved	4A	0.600V	8A	1.112V	CA	Reserved
0B	Reserved	4B	0.608V	8B	1.120V	CB	Reserved
0C	Reserved	4C	0.616V	8C	1.128V	CC	Reserved
0D	Reserved	4D	0.624V	8D	1.136V	CD	Reserved
0E	Reserved	4E	0.632V	8E	1.144V	CE	Reserved
0F	Reserved	4F	0.640V	8F	1.152V	CF	Reserved
10	Reserved	50	0.648V	90	1.160V	D0	Reserved
11	Reserved	51	0.656V	91	1.168V	D1	Reserved
12	Reserved	52	0.664V	92	1.176V	D2	Reserved
13	Reserved	53	0.672V	93	1.184V	D3	Reserved
14	Reserved	54	0.680V	94	1.192V	D4	Reserved
15	Reserved	55	0.688V	**95**	**1.200V**	D5	Reserved
16	Reserved	56	0.696V	96	1.208V	D6	Reserved
17	Reserved	57	0.704V	97	1.216V	D7	Reserved
18	Reserved	58	0.712V	98	1.224V	D8	Reserved
19	Reserved	59	0.720V	99	1.232V	D9	Reserved
1A	Reserved	5A	0.728V	9A	1.240V	DA	Reserved
1B	Reserved	5B	0.736V	9B	1.248V	DB	Reserved
1C	Reserved	5C	0.744V	9C	1.256V	DC	Reserved
1D	Reserved	5D	0.752V	9D	1.264V	DD	Reserved

7:0	LDO2_ VOUT	0000 0000	R/W	1E	Reserved	5E	0.760V	9E	1.272V	DE	Reserved
				1F	Reserved	5F	0.768V	9F	1.280V	DF	Reserved
				20	Reserved	60	0.776V	A0	1.288V	E0	Reserved
				21	Reserved	61	0.784V	A1	1.296V	E1	Reserved
				22	Reserved	62	0.792V	A2	1.304V	E2	Reserved
				23	Reserved	63	0.800V	A3	1.312V	E3	Reserved
				24	Reserved	64	0.808V	A4	1.320V	E4	Reserved
				25	Reserved	65	0.816V	A5	1.328V	E5	Reserved
				26	Reserved	66	0.824V	A6	1.336V	E6	Reserved
				27	Reserved	67	0.832V	A7	1.344V	E7	Reserved
				28	Reserved	68	0.840V	A8	1.352V	E8	Reserved
				29	Reserved	69	0.848V	A9	1.360V	E9	Reserved
				2A	Reserved	6A	0.856V	AA	1.368V	EA	Reserved
				2B	Reserved	6B	0.864V	AB	1.376V	EB	Reserved
				2C	Reserved	6C	0.872V	AC	1.384V	EC	Reserved
				2D	Reserved	6D	0.880V	AD	1.392V	ED	Reserved
				2E	Reserved	6E	0.888V	AE	1.400V	EE	Reserved
				2F	Reserved	6F	0.896V	AF	1.408V	EF	Reserved
				30	Reserved	70	0.904V	B0	1.416V	F0	Reserved
				31	Reserved	71	0.912V	B1	1.424V	F1	Reserved
				32	Reserved	72	0.920V	B2	1.432V	F2	Reserved
				33	Reserved	73	0.928V	B3	1.440V	F3	Reserved
				34	Reserved	74	0.936V	B4	1.448V	F4	Reserved
				35	Reserved	75	0.944V	B5	1.456V	F5	Reserved
				36	Reserved	76	0.952V	B6	1.464V	F6	Reserved
				37	Reserved	77	0.960V	B7	1.472V	F7	Reserved
				38	Reserved	78	0.968V	B8	1.480V	F8	Reserved
				39	Reserved	79	0.976V	B9	1.488V	F9	Reserved
				3A	Reserved	7A	0.984V	BA	1.496V	FA	Reserved
				3B	Reserved	7B	0.992V	BB	1.504V	FB	Reserved
				3C	Reserved	7C	1.000V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008V	BD	Reserved	FD	Reserved
				3E	0.504V	7E	1.016V	BE	Reserved	FE	Reserved
				3F	0.512V	7F	1.024V	BF	Reserved	FF	Reserved

REGISTER DETAILS – 0x06 LDO3

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO3_ VOUT	0000 0000	R/W	Sets LDO3 regulation target voltage. Equation: V_{OUT} =1.500V + [(d − 16) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884V	80	2.396V	C0	2.908V
1	Reserved	41	1.892V	81	2.404V	C1	2.916V
2	Reserved	42	1.900V	82	2.412V	C2	2.924V
3	Reserved	43	1.908V	83	2.420V	C3	2.932V
4	Reserved	44	1.916V	84	2.428V	C4	2.940V
5	Reserved	45	1.924V	85	2.436V	C5	2.948V
6	Reserved	46	1.932V	86	2.444V	C6	2.956V
7	Reserved	47	1.940V	87	2.452V	C7	2.964V
8	Reserved	48	1.948V	88	2.460V	C8	2.972V
9	Reserved	49	1.956V	89	2.468V	C9	2.980V
0A	Reserved	4A	1.964V	8A	2.476V	CA	2.988V
0B	Reserved	4B	1.972V	8B	2.484V	CB	2.996V
0C	Reserved	4C	1.980V	8C	2.492V	CC	3.004V
0D	Reserved	4D	1.988V	8D	2.500V	CD	3.012V
0E	Reserved	4E	1.996V	8E	2.508V	CE	3.020V
0F	Reserved	4F	2.004V	8F	2.516V	CF	3.028V
10	1.500V	50	2.012V	90	2.524V	D0	3.036V
11	1.508V	51	2.020V	91	2.532V	D1	3.044V
12	1.516V	52	2.028V	92	2.540V	D2	3.052V
13	1.524V	53	2.036V	93	2.548V	D3	3.060V
14	1.532V	54	2.044V	94	2.556V	D4	3.068V
15	1.540V	55	2.052V	95	2.564V	D5	3.076V
16	1.548V	56	2.060V	96	2.572V	D6	3.084V
17	1.556V	57	2.068V	97	2.580V	D7	3.092V
18	1.564V	58	2.076V	98	2.588V	D8	3.100V
19	1.572V	59	2.084V	99	2.596V	D9	3.108V
1A	1.580V	5A	2.092V	9A	2.604V	DA	3.116V
1B	1.588V	5B	2.100V	9B	2.612V	DB	3.124V
1C	1.596V	5C	2.108V	9C	2.620V	DC	3.132V
1D	1.604V	5D	2.116V	9D	2.628V	DD	3.140V

7:0	LDO3_ VOUT	0000 0000	R/W	1E	1.612V	5E	2.124V	9E	2.636V	DE	3.148V
				1F	1.620V	5F	2.132V	9F	2.644V	DF	3.156V
				20	1.628V	60	2.140V	A0	2.652V	E0	3.164V
				21	1.636V	61	2.148V	A1	2.660V	E1	3.172V
				22	1.644V	62	2.156V	A2	2.668V	E2	3.180V
				23	1.652V	63	2.164V	A3	2.676V	E3	3.188V
				24	1.660V	64	2.172V	A4	2.684V	E4	3.196V
				25	1.668V	65	2.180V	A5	2.692V	E5	3.204V
				26	1.676V	66	2.188V	A6	2.700V	E6	3.212V
				27	1.684V	67	2.196V	A7	2.708V	E7	3.220V
				28	1.692V	68	2.204V	A8	2.716V	E8	3.228V
				29	1.700V	69	2.212V	A9	2.724V	E9	3.236V
				2A	1.708V	6A	2.220V	AA	2.732V	EA	3.244V
				2B	1.716V	6B	2.228V	AB	2.740V	EB	3.252V
				2C	1.724V	6C	2.236V	AC	2.748V	EC	3.260V
				2D	1.732V	6D	2.244V	AD	2.756V	ED	3.268V
				2E	1.740V	6E	2.252V	AE	2.764V	EE	3.276V
				2F	1.748V	6F	2.260V	AF	2.772V	EF	3.284V
				30	1.756V	70	2.268V	B0	2.780V	F0	3.292V
				31	1.764V	71	2.276V	B1	2.788V	F1	3.300V
				32	1.772V	72	2.284V	B2	2.796V	F2	3.308V
				33	1.780V	73	2.292V	**B3**	**2.804V**	F3	3.316V
				34	1.788V	74	2.300V	B4	2.812V	F4	3.324V
				35	1.796V	75	2.308V	B5	2.820V	F5	3.332V
				36	1.804V	76	2.316V	B6	2.828V	F6	3.340V
				37	1.812V	77	2.324V	B7	2.836V	F7	3.348V
				38	1.820V	78	2.332V	B8	2.844V	F8	3.356V
				39	1.828V	79	2.340V	B9	2.852V	F9	3.364V
				3A	1.836V	7A	2.348V	BA	2.860V	FA	3.372V
				3B	1.844V	7B	2.356V	BB	2.868V	FB	3.380V
				3C	1.852V	7C	2.364V	BC	2.876V	FC	3.388V
				3D	1.860V	7D	2.372V	BD	2.884V	FD	3.396V
				3E	1.868V	7E	2.380V	BE	2.892V	FE	3.404V
				3F	1.876V	7F	2.388V	BF	2.900V	FF	3.412V

REGISTER DETAILS – 0x07 LDO4

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO4_ VOUT	0000 0000	R/W	Sets LDO4 regulation target voltage. Equation: V_{OUT} =1.500V + [(d − 16) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884V	80	2.396V	C0	2.908V
1	Reserved	41	1.892V	81	2.404V	C1	2.916V
2	Reserved	42	1.900V	82	2.412V	C2	2.924V
3	Reserved	43	1.908V	83	2.420V	C3	2.932V
4	Reserved	44	1.916V	84	2.428V	C4	2.940V
5	Reserved	45	1.924V	85	2.436V	C5	2.948V
6	Reserved	46	1.932V	86	2.444V	C6	2.956V
7	Reserved	47	1.940V	87	2.452V	C7	2.964V
8	Reserved	48	1.948V	88	2.460V	C8	2.972V
9	Reserved	49	1.956V	89	2.468V	C9	2.980V
0A	Reserved	4A	1.964V	8A	2.476V	CA	2.988V
0B	Reserved	4B	1.972V	8B	2.484V	CB	2.996V
0C	Reserved	4C	1.980V	8C	2.492V	CC	3.004V
0D	Reserved	4D	1.988V	8D	2.500V	CD	3.012V
0E	Reserved	4E	1.996V	8E	2.508V	CE	3.020V
0F	Reserved	4F	2.004V	8F	2.516V	CF	3.028V
10	1.500V	50	2.012V	90	2.524V	D0	3.036V
11	1.508V	51	2.020V	91	2.532V	D1	3.044V
12	1.516V	52	2.028V	92	2.540V	D2	3.052V
13	1.524V	53	2.036V	93	2.548V	D3	3.060V
14	1.532V	54	2.044V	94	2.556V	D4	3.068V
15	1.540V	55	2.052V	95	2.564V	D5	3.076V
16	1.548V	56	2.060V	96	2.572V	D6	3.084V
17	1.556V	57	2.068V	97	2.580V	D7	3.092V
18	1.564V	58	2.076V	98	2.588V	D8	3.100V
19	1.572V	59	2.084V	99	2.596V	D9	3.108V
1A	1.580V	5A	2.092V	9A	2.604V	DA	3.116V
1B	1.588V	5B	2.100V	9B	2.612V	DB	3.124V
1C	1.596V	5C	2.108V	9C	2.620V	DC	3.132V
1D	1.604V	5D	2.116V	9D	2.628V	DD	3.140V

7:0	LDO4_ VOUT	0000 0000	R/W	1E	1.612V	5E	2.124V	9E	2.636V	DE	3.148V
				1F	1.620V	5F	2.132V	9F	2.644V	DF	3.156V
				20	1.628V	60	2.140V	A0	2.652V	E0	3.164V
				21	1.636V	61	2.148V	A1	2.660V	E1	3.172V
				22	1.644V	62	2.156V	A2	2.668V	E2	3.180V
				23	1.652V	63	2.164V	A3	2.676V	E3	3.188V
				24	1.660V	64	2.172V	A4	2.684V	E4	3.196V
				25	1.668V	65	2.180V	A5	2.692V	E5	3.204V
				26	1.676V	66	2.188V	A6	2.700V	E6	3.212V
				27	1.684V	67	2.196V	A7	2.708V	E7	3.220V
				28	1.692V	68	2.204V	A8	2.716V	E8	3.228V
				29	1.700V	69	2.212V	A9	2.724V	E9	3.236V
				2A	1.708V	6A	2.220V	AA	2.732V	EA	3.244V
				2B	1.716V	6B	2.228V	AB	2.740V	EB	3.252V
				2C	1.724V	6C	2.236V	AC	2.748V	EC	3.260V
				2D	1.732V	6D	2.244V	AD	2.756V	ED	3.268V
				2E	1.740V	6E	2.252V	AE	2.764V	EE	3.276V
				2F	1.748V	6F	2.260V	AF	2.772V	EF	3.284V
				30	1.756V	70	2.268V	B0	2.780V	F0	3.292V
				31	1.764V	71	2.276V	B1	2.788V	F1	3.300V
				32	1.772V	72	2.284V	B2	2.796V	F2	3.308V
				33	1.780V	73	2.292V	**B3**	**2.804V**	F3	3.316V
				34	1.788V	74	2.300V	B4	2.812V	F4	3.324V
				35	1.796V	75	2.308V	B5	2.820V	F5	3.332V
				36	1.804V	76	2.316V	B6	2.828V	F6	3.340V
				37	1.812V	77	2.324V	B7	2.836V	F7	3.348V
				38	1.820V	78	2.332V	B8	2.844V	F8	3.356V
				39	1.828V	79	2.340V	B9	2.852V	F9	3.364V
				3A	1.836V	7A	2.348V	BA	2.860V	FA	3.372V
				3B	1.844V	7B	2.356V	BB	2.868V	FB	3.380V
				3C	1.852V	7C	2.364V	BC	2.876V	FC	3.388V
				3D	1.860V	7D	2.372V	BD	2.884V	FD	3.396V
				3E	1.868V	7E	2.380V	BE	2.892V	FE	3.404V
				3F	1.876V	7F	2.388V	BF	2.900V	FF	3.412V

REGISTER DETAILS – 0x08 LDO5

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO5_ VOUT	0000 0000	R/W	Sets LDO5 regulation target voltage. Equation: V_{OUT} =1.500V + [(d − 16) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884V	80	2.396V	C0	2.908V
1	Reserved	41	1.892V	81	2.404V	C1	2.916V
2	Reserved	42	1.900V	82	2.412V	C2	2.924V
3	Reserved	43	1.908V	83	2.420V	C3	2.932V
4	Reserved	44	1.916V	84	2.428V	C4	2.940V
5	Reserved	45	1.924V	85	2.436V	C5	2.948V
6	Reserved	46	1.932V	86	2.444V	C6	2.956V
7	Reserved	47	1.940V	87	2.452V	C7	2.964V
8	Reserved	48	1.948V	88	2.460V	C8	2.972V
9	Reserved	49	1.956V	89	2.468V	C9	2.980V
0A	Reserved	4A	1.964V	8A	2.476V	CA	2.988V
0B	Reserved	4B	1.972V	8B	2.484V	CB	2.996V
0C	Reserved	4C	1.980V	8C	2.492V	CC	3.004V
0D	Reserved	4D	1.988V	8D	2.500V	CD	3.012V
0E	Reserved	4E	1.996V	8E	2.508V	CE	3.020V
0F	Reserved	4F	2.004V	8F	2.516V	CF	3.028V
10	1.500V	50	2.012V	90	2.524V	D0	3.036V
11	1.508V	51	2.020V	91	2.532V	D1	3.044V
12	1.516V	52	2.028V	92	2.540V	D2	3.052V
13	1.524V	53	2.036V	93	2.548V	D3	3.060V
14	1.532V	54	2.044V	94	2.556V	D4	3.068V
15	1.540V	55	2.052V	95	2.564V	D5	3.076V
16	1.548V	56	2.060V	96	2.572V	D6	3.084V
17	1.556V	57	2.068V	97	2.580V	D7	3.092V
18	1.564V	58	2.076V	98	2.588V	D8	3.100V
19	1.572V	59	2.084V	99	2.596V	D9	3.108V
1A	1.580V	5A	2.092V	9A	2.604V	DA	3.116V
1B	1.588V	5B	2.100V	9B	2.612V	DB	3.124V
1C	1.596V	5C	2.108V	9C	2.620V	DC	3.132V
1D	1.604V	5D	2.116V	9D	2.628V	DD	3.140V

7:0	LDO5_ VOUT	0000 0000	R/W	1E	1.612V	5E	2.124V	9E	2.636V	DE	3.148V
				1F	1.620V	5F	2.132V	9F	2.644V	DF	3.156V
				20	1.628V	60	2.140V	A0	2.652V	E0	3.164V
				21	1.636V	61	2.148V	A1	2.660V	E1	3.172V
				22	1.644V	62	2.156V	A2	2.668V	E2	3.180V
				23	1.652V	63	2.164V	A3	2.676V	E3	3.188V
				24	1.660V	64	2.172V	A4	2.684V	E4	3.196V
				25	1.668V	65	2.180V	A5	2.692V	E5	3.204V
				26	1.676V	66	2.188V	A6	2.700V	E6	3.212V
				27	1.684V	67	2.196V	A7	2.708V	E7	3.220V
				28	1.692V	68	2.204V	A8	2.716V	E8	3.228V
				29	1.700V	69	2.212V	A9	2.724V	E9	3.236V
				2A	1.708V	6A	2.220V	AA	2.732V	EA	3.244V
				2B	1.716V	6B	2.228V	AB	2.740V	EB	3.252V
				2C	1.724V	6C	2.236V	AC	2.748V	EC	3.260V
				2D	1.732V	6D	2.244V	AD	2.756V	ED	3.268V
				2E	1.740V	6E	2.252V	AE	2.764V	EE	3.276V
				2F	1.748V	6F	2.260V	AF	2.772V	EF	3.284V
				30	1.756V	70	2.268V	B0	2.780V	F0	3.292V
				31	1.764V	71	2.276V	B1	2.788V	F1	3.300V
				32	1.772V	72	2.284V	B2	2.796V	F2	3.308V
				33	1.780V	73	2.292V	**B3**	**2.804V**	F3	3.316V
				34	1.788V	74	2.300V	B4	2.812V	F4	3.324V
				35	1.796V	75	2.308V	B5	2.820V	F5	3.332V
				36	1.804V	76	2.316V	B6	2.828V	F6	3.340V
				37	1.812V	77	2.324V	B7	2.836V	F7	3.348V
				38	1.820V	78	2.332V	B8	2.844V	F8	3.356V
				39	1.828V	79	2.340V	B9	2.852V	F9	3.364V
				3A	1.836V	7A	2.348V	BA	2.860V	FA	3.372V
				3B	1.844V	7B	2.356V	BB	2.868V	FB	3.380V
				3C	1.852V	7C	2.364V	BC	2.876V	FC	3.388V
				3D	1.860V	7D	2.372V	BD	2.884V	FD	3.396V
				3E	1.868V	7E	2.380V	BE	2.892V	FE	3.404V
				3F	1.876V	7F	2.388V	BF	2.900V	FF	3.412V

REGISTER DETAILS – 0x09 LDO6

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO6_ VOUT	0000 0000	R/W	Sets LDO6 regulation target voltage. Equation: V_{OUT} =1.500V + [(d − 16) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884V	80	2.396V	C0	2.908V
1	Reserved	41	1.892V	81	2.404V	C1	2.916V
2	Reserved	42	1.900V	82	2.412V	C2	2.924V
3	Reserved	43	1.908V	83	2.420V	C3	2.932V
4	Reserved	44	1.916V	84	2.428V	C4	2.940V
5	Reserved	45	1.924V	85	2.436V	C5	2.948V
6	Reserved	46	1.932V	86	2.444V	C6	2.956V
7	Reserved	47	1.940V	87	2.452V	C7	2.964V
8	Reserved	48	1.948V	88	2.460V	C8	2.972V
9	Reserved	49	1.956V	89	2.468V	C9	2.980V
0A	Reserved	4A	1.964V	8A	2.476V	CA	2.988V
0B	Reserved	4B	1.972V	8B	2.484V	CB	2.996V
0C	Reserved	4C	1.980V	8C	2.492V	CC	3.004V
0D	Reserved	4D	1.988V	8D	2.500V	CD	3.012V
0E	Reserved	4E	1.996V	8E	2.508V	CE	3.020V
0F	Reserved	4F	2.004V	8F	2.516V	CF	3.028V
10	1.500V	50	2.012V	90	2.524V	D0	3.036V
11	1.508V	51	2.020V	91	2.532V	D1	3.044V
12	1.516V	52	2.028V	92	2.540V	D2	3.052V
13	1.524V	53	2.036V	93	2.548V	D3	3.060V
14	1.532V	54	2.044V	94	2.556V	D4	3.068V
15	1.540V	55	2.052V	95	2.564V	D5	3.076V
16	1.548V	56	2.060V	96	2.572V	D6	3.084V
17	1.556V	57	2.068V	97	2.580V	D7	3.092V
18	1.564V	58	2.076V	98	2.588V	D8	3.100V
19	1.572V	59	2.084V	99	2.596V	D9	3.108V
1A	1.580V	5A	2.092V	9A	2.604V	DA	3.116V
1B	1.588V	5B	2.100V	9B	2.612V	DB	3.124V
1C	1.596V	5C	2.108V	9C	2.620V	DC	3.132V
1D	1.604V	5D	2.116V	9D	2.628V	DD	3.140V

7:0	LDO6_ VOUT	0000 0000	R/W	1E	1.612V	5E	2.124V	9E	2.636V	DE	3.148V
				1F	1.620V	5F	2.132V	9F	2.644V	DF	3.156V
				20	1.628V	60	2.140V	A0	2.652V	E0	3.164V
				21	1.636V	61	2.148V	A1	2.660V	E1	3.172V
				22	1.644V	62	2.156V	A2	2.668V	E2	3.180V
				23	1.652V	63	2.164V	A3	2.676V	E3	3.188V
				24	1.660V	64	2.172V	A4	2.684V	E4	3.196V
				25	1.668V	65	2.180V	A5	2.692V	E5	3.204V
				26	1.676V	66	2.188V	A6	2.700V	E6	3.212V
				27	1.684V	67	2.196V	A7	2.708V	E7	3.220V
				28	1.692V	68	2.204V	A8	2.716V	E8	3.228V
				29	1.700V	69	2.212V	A9	2.724V	E9	3.236V
				2A	1.708V	6A	2.220V	AA	2.732V	EA	3.244V
				2B	1.716V	6B	2.228V	AB	2.740V	EB	3.252V
				2C	1.724V	6C	2.236V	AC	2.748V	EC	3.260V
				2D	1.732V	6D	2.244V	AD	2.756V	ED	3.268V
				2E	1.740V	6E	2.252V	AE	2.764V	EE	3.276V
				2F	1.748V	6F	2.260V	AF	2.772V	EF	3.284V
				30	1.756V	70	2.268V	B0	2.780V	F0	3.292V
				31	1.764V	71	2.276V	B1	2.788V	F1	3.300V
				32	1.772V	72	2.284V	B2	2.796V	F2	3.308V
				33	1.780V	73	2.292V	**B3**	**2.804V**	F3	3.316V
				34	1.788V	74	2.300V	B4	2.812V	F4	3.324V
				35	1.796V	75	2.308V	B5	2.820V	F5	3.332V
				36	1.804V	76	2.316V	B6	2.828V	F6	3.340V
				37	1.812V	77	2.324V	B7	2.836V	F7	3.348V
				38	1.820V	78	2.332V	B8	2.844V	F8	3.356V
				39	1.828V	79	2.340V	B9	2.852V	F9	3.364V
				3A	1.836V	7A	2.348V	BA	2.860V	FA	3.372V
				3B	1.844V	7B	2.356V	BB	2.868V	FB	3.380V
				3C	1.852V	7C	2.364V	BC	2.876V	FC	3.388V
				3D	1.860V	7D	2.372V	BD	2.884V	FD	3.396V
				3E	1.868V	7E	2.380V	BE	2.892V	FE	3.404V
				3F	1.876V	7F	2.388V	BF	2.900V	FF	3.412V

REGISTER DETAILS – 0x0A LDO7

Default = 10110011

Bits	Name	Default	Type	Description
7:0	LDO7_ VOUT	0000 0000	R/W	Sets LDO7 regulation target voltage. Equation: V_{OUT} =1.500V + [(d − 16) x 8mV], where d is the decimal value of the register

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
0	Reserved	40	1.884V	80	2.396V	C0	2.908V
1	Reserved	41	1.892V	81	2.404V	C1	2.916V
2	Reserved	42	1.900V	82	2.412V	C2	2.924V
3	Reserved	43	1.908V	83	2.420V	C3	2.932V
4	Reserved	44	1.916V	84	2.428V	C4	2.940V
5	Reserved	45	1.924V	85	2.436V	C5	2.948V
6	Reserved	46	1.932V	86	2.444V	C6	2.956V
7	Reserved	47	1.940V	87	2.452V	C7	2.964V
8	Reserved	48	1.948V	88	2.460V	C8	2.972V
9	Reserved	49	1.956V	89	2.468V	C9	2.980V
0A	Reserved	4A	1.964V	8A	2.476V	CA	2.988V
0B	Reserved	4B	1.972V	8B	2.484V	CB	2.996V
0C	Reserved	4C	1.980V	8C	2.492V	CC	3.004V
0D	Reserved	4D	1.988V	8D	2.500V	CD	3.012V
0E	Reserved	4E	1.996V	8E	2.508V	CE	3.020V
0F	Reserved	4F	2.004V	8F	2.516V	CF	3.028V
10	1.500V	50	2.012V	90	2.524V	D0	3.036V
11	1.508V	51	2.020V	91	2.532V	D1	3.044V
12	1.516V	52	2.028V	92	2.540V	D2	3.052V
13	1.524V	53	2.036V	93	2.548V	D3	3.060V
14	1.532V	54	2.044V	94	2.556V	D4	3.068V
15	1.540V	55	2.052V	95	2.564V	D5	3.076V
16	1.548V	56	2.060V	96	2.572V	D6	3.084V
17	1.556V	57	2.068V	97	2.580V	D7	3.092V
18	1.564V	58	2.076V	98	2.588V	D8	3.100V
19	1.572V	59	2.084V	99	2.596V	D9	3.108V
1A	1.580V	5A	2.092V	9A	2.604V	DA	3.116V
1B	1.588V	5B	2.100V	9B	2.612V	DB	3.124V
1C	1.596V	5C	2.108V	9C	2.620V	DC	3.132V
1D	1.604V	5D	2.116V	9D	2.628V	DD	3.140V

7:0	LDO7_ VOUT	0000 0000	R/W	1E	1.612V	5E	2.124V	9E	2.636V	DE	3.148V
				1F	1.620V	5F	2.132V	9F	2.644V	DF	3.156V
				20	1.628V	60	2.140V	A0	2.652V	E0	3.164V
				21	1.636V	61	2.148V	A1	2.660V	E1	3.172V
				22	1.644V	62	2.156V	A2	2.668V	E2	3.180V
				23	1.652V	63	2.164V	A3	2.676V	E3	3.188V
				24	1.660V	64	2.172V	A4	2.684V	E4	3.196V
				25	1.668V	65	2.180V	A5	2.692V	E5	3.204V
				26	1.676V	66	2.188V	A6	2.700V	E6	3.212V
				27	1.684V	67	2.196V	A7	2.708V	E7	3.220V
				28	1.692V	68	2.204V	A8	2.716V	E8	3.228V
				29	1.700V	69	2.212V	A9	2.724V	E9	3.236V
				2A	1.708V	6A	2.220V	AA	2.732V	EA	3.244V
				2B	1.716V	6B	2.228V	AB	2.740V	EB	3.252V
				2C	1.724V	6C	2.236V	AC	2.748V	EC	3.260V
				2D	1.732V	6D	2.244V	AD	2.756V	ED	3.268V
				2E	1.740V	6E	2.252V	AE	2.764V	EE	3.276V
				2F	1.748V	6F	2.260V	AF	2.772V	EF	3.284V
				30	1.756V	70	2.268V	B0	2.780V	F0	3.292V
				31	1.764V	71	2.276V	B1	2.788V	F1	3.300V
				32	1.772V	72	2.284V	B2	2.796V	F2	3.308V
				33	1.780V	73	2.292V	**B3**	**2.804V**	F3	3.316V
				34	1.788V	74	2.300V	B4	2.812V	F4	3.324V
				35	1.796V	75	2.308V	B5	2.820V	F5	3.332V
				36	1.804V	76	2.316V	B6	2.828V	F6	3.340V
				37	1.812V	77	2.324V	B7	2.836V	F7	3.348V
				38	1.820V	78	2.332V	B8	2.844V	F8	3.356V
				39	1.828V	79	2.340V	B9	2.852V	F9	3.364V
				3A	1.836V	7A	2.348V	BA	2.860V	FA	3.372V
				3B	1.844V	7B	2.356V	BB	2.868V	FB	3.380V
				3C	1.852V	7C	2.364V	BC	2.876V	FC	3.388V
				3D	1.860V	7D	2.372V	BD	2.884V	FD	3.396V
				3E	1.868V	7E	2.380V	BE	2.892V	FE	3.404V
				3F	1.876V	7F	2.388V	BF	2.900V	FF	3.412V

REGISTER DETAILS – 0x0B LDO12_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO2_SEQ	000	R/W	The LDO2 sequencing is selected by setting bits [5:3].

Code	Slot Selected
000	Controlled through I²C by setting the LDO2_EN bit
001	Selects slot 1 for the LDO2 to be enabled in at power up
010	Selects slot 2 for the LDO2 to be enabled in at power up
011	Selects slot 3 for the LDO2 to be enabled in at power up
100	Selects slot 4 for the LDO2 to be enabled in at power up
101	Selects slot 5 for the LDO2 to be enabled in at power up
110	Selects slot 6 for the LDO2 to be enabled in at power up
111	Selects slot 7 for the LDO2 to be enabled in at power up

Bits	Name	Default	Type	Description
2:0	LDO1_SEQ	000	R/W	The LDO1 sequencing is selected by setting bits [2:0].

Code	Slot Selected
000	Controlled through I²C by setting the LDO1_EN bit
001	Selects slot 1 for the LDO1 to be enabled in at power up
010	Selects slot 2 for the LDO1 to be enabled in at power up
011	Selects slot 3 for the LDO1 to be enabled in at power up
100	Selects slot 4 for the LDO1 to be enabled in at power up
101	Selects slot 5 for the LDO1 to be enabled in at power up
110	Selects slot 6 for the LDO1 to be enabled in at power up
111	Selects slot 7 for the LDO1 to be enabled in at power up

REGISTER DETAILS – 0x0C LDO34_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO4_SEQ	000	R/W	The LDO4 sequencing is selected by setting bits [5:3].

Code	Slot Selected
000	Controlled through I²C by setting the LDO4_EN bit
001	Selects slot 1 for the LDO4 to be enabled in at power up
010	Selects slot 2 for the LDO4 to be enabled in at power up
011	Selects slot 3 for the LDO4 to be enabled in at power up
100	Selects slot 4 for the LDO4 to be enabled in at power up
101	Selects slot 5 for the LDO4 to be enabled in at power up
110	Selects slot 6 for the LDO4 to be enabled in at power up
111	Selects slot 7 for the LDO4 to be enabled in at power up

Bits	Name	Default	Type	Description
2:0	LDO3_SEQ	000	R/W	The LDO3 sequencing is selected by setting bits [2:0].

Code	Slot Selected
000	Controlled through I²C by setting the LDO3_EN bit
001	Selects slot 1 for the LDO3 to be enabled in at power up
010	Selects slot 2 for the LDO3 to be enabled in at power up
011	Selects slot 3 for the LDO3 to be enabled in at power up
100	Selects slot 4 for the LDO3 to be enabled in at power up
101	Selects slot 5 for the LDO3 to be enabled in at power up
110	Selects slot 6 for the LDO3 to be enabled in at power up
111	Selects slot 7 for the LDO3 to be enabled in at power up

REGISTER DETAILS – 0x0D LDO56_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO6_SEQ	000	R/W	The LDO6 sequencing is selected by setting bits [5:3]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO6_EN bit 001 – Selects slot 1 for the LDO6 to be enabled in at power up 010 – Selects slot 2 for the LDO6 to be enabled in at power up 011 – Selects slot 3 for the LDO6 to be enabled in at power up 100 – Selects slot 4 for the LDO6 to be enabled in at power up 101 – Selects slot 5 for the LDO6 to be enabled in at power up 110 – Selects slot 6 for the LDO6 to be enabled in at power up 111 – Selects slot 7 for the LDO6 to be enabled in at power up
2:0	LDO5_SEQ	000	R/W	The LDO5 sequencing is selected by setting bits [2:0]. **Code** – **Slot Selected** 000 – Controlled through I²C by setting the LDO5_EN bit 001 – Selects slot 1 for the LDO5 to be enabled in at power up 010 – Selects slot 2 for the LDO5 to be enabled in at power up 011 – Selects slot 3 for the LDO5 to be enabled in at power up 100 – Selects slot 4 for the LDO5 to be enabled in at power up 101 – Selects slot 5 for the LDO5 to be enabled in at power up 110 – Selects slot 6 for the LDO5 to be enabled in at power up 111 – Selects slot 7 for the LDO5 to be enabled in at power up

REGISTER DETAILS – 0x0E LDO7_SEQ

Default = 00000000

Bits	Name	Default	Type	Description
7:6	UNUSED			
5:3	LDO7_SEQ	000	R/W	The LDO7 sequencing is selected by setting bits [5:3].

Code	Slot Selected
000	Controlled through I²C by setting the LDO7_EN bit
001	Selects slot 1 for the LDO7 to be enabled in at power up
010	Selects slot 2 for the LDO7 to be enabled in at power up
011	Selects slot 3 for the LDO7 to be enabled in at power up
100	Selects slot 4 for the LDO7 to be enabled in at power up
101	Selects slot 5 for the LDO7 to be enabled in at power up
110	Selects slot 6 for the LDO7 to be enabled in at power up
111	Selects slot 7 for the LDO7 to be enabled in at power up

REGISTER DETAILS – 0x0F SEQUENCING

Default = 00000000

Bits	Name	Default	Type	Description	
7:6	SEQ_SPEED	00	R/W	**Code**	**Period per Slot**
				00	500 µs
				01	1.0 ms
				10	1.5 ms
				11	2.0 ms
5:4	SEQ_CONTROL	00	W/CLR	**Code**	**Initialize Power-Up or Power-Down**
				00	Default
				01	Starts an LDO power-up sequence.
				10	Starts an LDO shutdown sequence.
				11	Bit configuration is ignored.
3	SEQ_ON	0	Read	**Code**	**The Indicator of the of sequencer status. Read only.**
				0	Shut down
				1	Power up
2:0	SEQ_COUNT	000	Read	**Code**	**Present Slot**
				000	Indicates sequencing has completed or not started.
				001	Indicates was in slot 1 during register read.
				010	Indicates was in slot 2 during register read.
				011	Indicates was in slot 3 during register read.
				100	Indicates was in slot 4 during register read.
				101	Indicates was in slot 5 during register read.
				110	Indicates was in slot 6 during register read.
				111	Indicates was in slot 7 during register read.

REGISTER DETAILS – 0x10 DISCHARGE

Default = 01111111

Bits	Name	Default	Type	Description	
7	UNUSED	0			
6	LDO1_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO1 Active Discharge feature is disabled. Pull−down will not be activated when LDO1 is disabled by any event.
				1	LDO1 Active Discharge feature is enabled. Pull−down will be activated when LDO1 is disabled by RESET_B going low or LDO1_EN = 0 or a sequenced shutdown or in a UVP event.
5	LDO2_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO2 Active Discharge feature is disabled. Pull−down will not be activated when LDO2 is disabled by any event.
				1	LDO2 Active Discharge feature is enabled. Pull−down will be activated when LDO2 is disabled by RESET_B going low or LDO2_EN = 0 or a sequenced shutdown or in a UVP event.
4	LDO3_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO3 Active Discharge feature is disabled. Pull−down will not be activated when LDO3 is disabled by any event.
				1	LDO3 Active Discharge feature is enabled. Pull−down will be activated when LDO3 is disabled by RESET_B going low or LDO3_EN = 0 or a sequenced shutdown or in a UVP event.
3	LDO4_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO4 Active Discharge feature is disabled. Pull−down will not be activated when LDO4 is disabled by any event.
				1	LDO4 Active Discharge feature is enabled. Pull−down will be activated when LDO4 is disabled by RESET_B going low or LDO4_EN = 0 or a sequenced shutdown or in a UVP event.
2	LDO5_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO5 Active Discharge feature is disabled. Pull−down will not be activated when LDO5 is disabled by any event.
				1	LDO5 Active Discharge feature is enabled. Pull−down will be activated when LDO5 is disabled by RESET_B going low or LDO5_EN = 0 or a sequenced shutdown or in a UVP event.
1	LDO6_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO6 Active Discharge feature is disabled. Pull−down will not be activated when LDO6 is disabled by any event.
				1	LDO6 Active Discharge feature is enabled. Pull−down will be activated when LDO6 is disabled by RESET_B going low or LDO6_EN = 0 or a sequenced shutdown or in a UVP event.

0	LDO7_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO7 Active Discharge feature is disabled. Pull−down will not be activated when LDO7 is disabled by any event.
				1	LDO7 Active Discharge feature is enabled. Pull−down will be activated when LDO7 is disabled by RESET_B going low or LDO7_EN = 0 or a sequenced shutdown or in a UVP event.

REGISTER DETAILS – 0x11 RESET

Default = 00000110

Bits	Name	Default	Type	Description	
7:4	SOFT_RESET	0000	Write	**Code**	**Software Reset**
				1011	Writing a ”1011” begins a soft reset of the device I²C registers to their default values. This bit is cleared upon the execution of the reset function.
					Any other value than “1011” will be ignored.
3	UNUSED				
2:1	OCP_TIMER	11	R/W	Option bits to control the length of the deglitch timer for the current limit on all LDOs before a fault is triggered.	
				Code	**Deglitch Timer**
				00	125 µs
				01	250 µs
				10	500 µs
				11	1 ms
0	FLT_SD_B	0	R/W	**Code**	**Prevents Shutdown when a Fault Occurs**
				0	LDO shuts down if a UVP or OCP event occurs or if the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event.
				1	LDO does not shut down if a UVP or OCP event occurs. If the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event, the associated LDO will shut down until the supply returns, but the fault will not be counted.
				NOTE: If this bit function is desired, FLT_SD_B should be set to ”1” prior to enabling any LDOs after a Power−On−Reset.	

REGISTER DETAILS – 0x12 12C_ADDR

Default = 10000001

Bits	Name	Default	Type	Description	
7	INT_LEVEL_SEL	0	R/W	**Code**	INT PUSH-PULL Output Level Select
				0	Output 1.8V when INT high
				1	Cutout 1.2V when INT high
6	INT_OutMode_SEL	0	R/W	**Code**	INT Output Mode Select
				0	Using PUSH-PULL for Output
				1	Using OPEN-DRAIN for Output
5:2	UNUSED		R/W		
1:0	I²C_ADDR_SEL	01	R/W	**Code**	**I²C Address Settings**
				00	0x20
				01	0x35
				10	0x61
				11	0x72

REGISTER DETAILS – 0x13, 0x14 RESERVED

REGISTER DETAILS – 0x15 INTERRUPT1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_UVP_INT	0	R/CLR	**Code**	**LDO7 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO7 output.
5	LDO6_UVP_INT	0	R/CLR	**Code**	**LDO6 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO6 output.
4	LDO5_UVP_INT	0	R/CLR	**Code**	**LDO5 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO5 output.
3	LDO4_UVP_INT	0	R/CLR	**Code**	**LDO4 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO4 output.
2	LDO3_UVP_INT	0	R/CLR	**Code**	**LDO3 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO3 output.

1	LDO2_UVP_INT	0	R/CLR	**Code**	**LDO2 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO2 output.
0	LDO1_UVP_INT	0	R/CLR	**Code**	**LDO1 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO1 output.

REGISTER DETAILS – 0x16 INTERRUPT2

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_OCP_INT	0	R/CLR	**Code**	**LDO7 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO7 output.
5	LDO6_OCP_INT	0	R/CLR	**Code**	**LDO6 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO6 output.
4	LDO5_OCP_INT	0	R/CLR	**Code**	**LDO5 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO5 output.
3	LDO4_OCP_INT	0	R/CLR	**Code**	**LDO4 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO4 output.
2	LDO3_OCP_INT	0	R/CLR	**Code**	**LDO3 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO3 output.
1	LDO2_OCP_INT	0	R/CLR	**Code**	**LDO2 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO2 output.
0	LDO1_OCP_INT	0	R/CLR	**Code**	**LDO1 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO1 output.

REGISTER DETAILS – 0x17 INTERRUPT3

Default = 00000000

Bits	Name	Default	Type	Description	
7	TSD_INT	0	R/CLR	**Code**	**Thermal Shutdown Interrupt**
				0	Clear
				1	A Thermal Shutdown event is detected or the temperature has fallen below the hysteresis level.
6	TSD_WRN_INT	0	R/CLR	**Code**	**Thermal Warning Interrupt**
				0	Clear
				1	The Thermal Shutdown Warning threshold was surpassed or the temperature has fallen below the hysteresis level.
5	VSYS_UVLO_INT	0	R/CLR	**Code**	**VSYS Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VSYS fell below the UVLO falling threshold or that VSYS have risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
4	LDO7_UVLO_INT	0	R/CLR	**Code**	**VIN7 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN7 fell below the UVLO falling threshold while LDO7 was enabled or VIN7 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
3	LDO6_UVLO_INT	0	R/CLR	**Code**	**VIN6 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN6 fell below the UVLO falling threshold while LDO6 was enabled or VIN6 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
2	LDO5_UVLO_INT	0	R/CLR	**Code**	**VIN5 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN5 fell below the UVLO falling threshold while LDO5 was enabled or VIN5 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
1	LDO34_UVLO_INT	0	R/CLR	**Code**	**VIN34 Under−Voltage−Lock−Out Interrupt**
				0	Clear

				1	VIN34 fell below the UVLO falling threshold while LDO3 and/or LDO4 were enabled or VIN34 has risen above the rising UVLO thresholds after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	
0	LDO12_UVLO_INT	0	R/CLR	**Code**	**VIN12 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN12 fell below the UVLO falling threshold while LDO1 and/or LDO2 were enabled or VIN12 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides the present state of the input voltage.	

REGISTER DETAILS – 0x18 STATUS1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_UVP_STAT	0	Read	**Code**	**LDO7 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO7 output.
5	LDO6_UVP_STAT	0	Read	**Code**	**LDO6 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO6 output.
4	LDO5_UVP_STAT	0	Read	**Code**	**LDO5 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO5 output.
3	LDO4_UVP_STAT	0	Read	**Code**	**LDO4 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO4 output.
2	LDO3_UVP_STAT	0	Read	**Code**	**LDO3 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO3 output.
1	LDO2_UVP_STAT	0	Read	**Code**	**LDO2 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO2 output.
0	LDO1_UVP_STAT	0	Read	**Code**	**LDO1 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO1 output.

REGISTER DETAILS – 0x19 STATUS2

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	LDO7_OCP_STAT	0	Read	**Code**	**LDO7 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO7 output.
5	LDO6_OCP_STAT	0	Read	**Code**	**LDO6 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO6 output.
4	LDO5_OCP_STAT	0	Read	**Code**	**LDO5 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO5 output.
3	LDO4_OCP_STAT	0	Read	**Code**	**LDO4 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO4 output.
2	LDO3_OCP_STAT	0	Read	**Code**	**LDO3 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO3 output.
1	LDO2_OCP_STAT	0	Read	**Code**	**LDO2 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO2 output.
0	LDO1_OCP_STAT	0	Read	**Code**	**LDO1 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO1 output.

REGISTER DETAILS – 0x1A STATUS3

Default = 00000000

Bits	Name	Default	Type	Description	
7	TSD_STAT	0	Read	**Code**	**Thermal Shutdown Status**
				0	Normal Operation
				1	Device is in Thermal Shutdown.
6	TSD_WRN_STAT	0	Read	**Code**	**Thermal Warning Status**
				0	Normal Operation
				1	The temperature is above the Thermal Warning level and shutdown is impending.
5	VSYS_UVLO_STAT	0	Read	**Code**	**VSYS Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VSYS is below the UVLO threshold.
4	LDO7_UVLO_STAT	0	Read	**Code**	**VIN7 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN7 is below the UVLO threshold while LDO7 is enabled.
3	LDO6_UVLO_STAT	0	Read	**Code**	**VIN6 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN6 is below the UVLO threshold while LDO6 is enabled.
2	LDO5_UVLO_STAT	0	Read	**Code**	**VIN5 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN5 is below the UVLO threshold while LDO5 is enabled.
1	LDO34_UVLO_STAT	0	Read	**Code**	**VIN34 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN34 is below the UVLO threshold while LDO3 and/or LDO4 are enabled.
0	LDO12_UVLO_STAT	0	Read	**Code**	**VIN12 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN12 is below the UVLO threshold while LDO1 and/or LDO2 are enabled.

REGISTER DETAILS – 0x1B STATUS4

Default = 00000000

Bits	Name	Default	Type	Description	
7	CHIP_SUSD	0	Read	**Code**	**Chip Suspension**
				0	Chip in normal state
				1	The entire chip has been suspended due to a global fault condition.
6	LDO7_SUSD	0	Read	**Code**	**LDO7 Output Suspended**
				0	LDO7 in normal state
				1	LDO7 has been suspended due to a fault condition.
5	LDO6_SUSD	0	Read	**Code**	**LDO6 Output Suspended**
				0	LDO6 in normal state
				1	LDO6 has been suspended due to a fault condition.
4	LDO5_SUSD	0	Read	**Code**	**LDO5 Output Suspended**
				0	LDO5 in normal state
				1	LDO5 has been suspended due to a fault condition.
3	LDO4_SUSD	0	Read	**Code**	**LDO4 Output Suspended**
				0	LDO4 in normal state
				1	LDO4 has been suspended due to a fault condition.
2	LDO3_SUSD	0	Read	**Code**	**LDO3 Output Suspended**
				0	LDO3 in normal state
				1	LDO3 has been suspended due to a fault condition.
1	LDO2_SUSD	0	Read	**Code**	**LDO2 Output Suspended**
				0	LDO2 in normal state
				1	LDO2 has been suspended due to a fault condition.
0	LDO1_SUSD	0	Read	**Code**	**LDO1 Output Suspended**
				0	LDO1 in normal state
				1	LDO1 has been suspended due to a fault condition.

REGISTER DETAILS – 0x1C MINT1

Default = 00000000

Bits	Name	Default	Type	Description	
7	UNUSED				
6	MASK_LDO7 _UVP	0	R/W	**Code**	**LDO7 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 Under−Voltage interrupt occurs.
5	MASK_LDO6 _UVP	0	R/W	**Code**	**LDO6 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 Under−Voltage interrupt occurs.
4	MASK_LDO5 _UVP	0	R/W	**Code**	**LDO5 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 Under−Voltage interrupt occurs.
3	MASK_LDO4 _UVP	0	R/W	**Code**	**LDO4 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 Under−Voltage interrupt occurs.
2	MASK_LDO3 _UVP	0	R/W	**Code**	**LDO3 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 Under−Voltage interrupt occurs.
1	MASK_LDO2 _UVP	0	R/W	**Code**	**LDO2 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 Under−Voltage interrupt occurs.
0	MASK_LDO1 _UVP	0	R/W	**Code**	**LDO1 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 Under−Voltage interrupt occurs.

REGISTER DETAILS – 0x1D MINT2

Default = 00000000

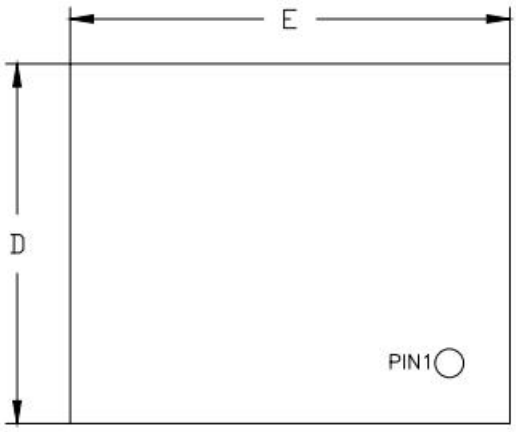
Bits	Name	Default	Type	Description	
7	UNUSED				
6	MASK_LDO7_OCP	0	R/W	**Code**	**LDO7 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 Over−Current interrupt occurs
5	MASK_LDO6_OCP	0	R/W	**Code**	**LDO6 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 Over−Current interrupt occurs
4	MASK_LDO5_OCP	0	R/W	**Code**	**LDO5 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 Over−Current interrupt occurs
3	MASK_LDO4_OCP	0	R/W	**Code**	**LDO4 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 Over−Current interrupt occurs
2	MASK_LDO3_OCP	0	R/W	**Code**	**LDO3 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 Over−Current interrupt occurs
1	MASK_LDO2_OCP	0	R/W	**Code**	**LDO2 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 Over−Current interrupt occurs
0	MASK_LDO1_OCP	0	R/W	**Code**	**LDO1 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 Over−Current interrupt occurs

REGISTER DETAILS – 0x1E MINT3

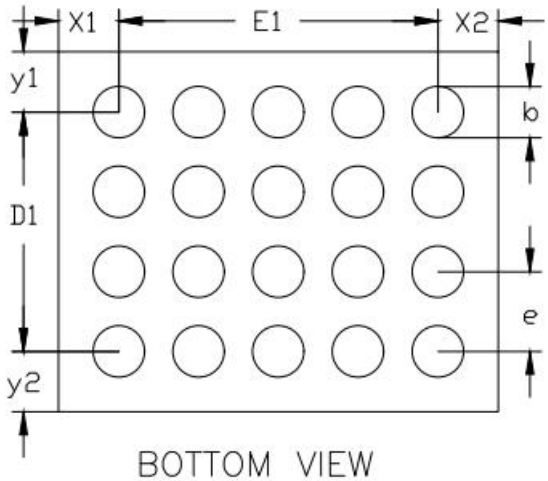
Default = 00000000

Bits	Name	Default	Type	Description	
7	MASK_TSD	0	R/W	**Code**	**Thermal Shutdown MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Shutdown interrupt occurs.
6	MASK_TSD_WRN	0	R/W	**Code**	**Thermal Warning MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Warning interrupt occurs.
5	MASK_VSYS_UVLO	0	R/W	**Code**	**VSYS UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VSYS Input Power Under−Voltage interrupt occurs.
4	MASK_LDO7_UVLO	0	R/W	**Code**	**LDO7 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN7 Input Power Under−Voltage interrupt occurs.
3	MASK_LDO6_UVLO	0	R/W	**Code**	**VIN6 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN6 Input Power Under−Voltage interrupt occurs.
2	MASK_LDO5_UVLO	0	R/W	**Code**	**VIN5 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN5 Input Power Under−Voltage interrupt occurs.
1	MASK_LDO34_UVLO	0	R/W	**Code**	**VIN34 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN34 Input Power Under−Voltage interrupt occurs.
0	MASK_LDO12_UVLO	0	R/W	**Code**	**VIN12 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN12 Input Power Under−Voltage interrupt occurs.

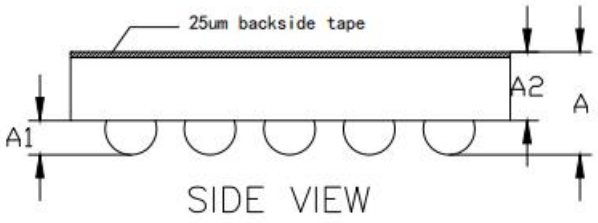
Physical Dimensions: WLCSP-20



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	**MIN**	**NOM**	**MAX**
A	0.410	0.450	0.490
A1	0.130	0.150	0.170
A2	0.280	0.300	0.320
D	1.550	1.580	1.610
D1		1.050BSC	
E	1.900	1.930	1.960
E1		1.400 BSC	
b	0.205	0.225	0.245
e		0.350 BSC	
x1		0.265 REF	
x2		0.265 REF	
y1		0.265 REF	
y2		0.265 REF	

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as cell phones, handheld products, laptops, medical equipment, and so on. Dioo's product families include analog signal processing and amplifying, LED drivers, and charger ICs. Go to http://www.dioo.com for a complete list of Dioo product families.

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