DIO7966
250 mA, Ultra-Low Noise and High PSRR LDO for RF and Analog Circuits

Features

- Operating input voltage range: 1.65 V to 5.5 V
- Available in fixed voltage option: 1 V to 3.3 V
- Output current：250 mA
- Ultra high PSRR: Typ. 95 dB at f = 1 kHz
- Ultra low noise: 10μV_{RMS}
- Output Voltage Accuracy: ±1%
- Ultra-low quiescent current: Typ. 18 μA
- Standby current: Typ. 0.1 μA
- Very low dropout: 100mV at 250 mA
- Stable with a 1 μF small case size ceramic capacitor
- Quick output discharge:
  DIO7966A: available
  DIO7966B: not available
- Small package: DFN1*1-4

Descriptions

The DIO7966 series is a 250 mA, ultra-high PSRR, ultra-low noise, high accuracy, low dropout CMOS Linear regulator with high ripple rejection. Designed for RF and analog circuits. The device consumes low quiescent current and provides fast line and load transient performance. The DIO7966 operates over an input voltage range of 1.65 V to 5.5 V and supports fixed output voltage of 3.3 V.

The DIO7966 is designed to work with a 1μF input and a 1 μF output ceramic capacitor, allowing for a small overall solution size. A precision band-gap and error amplifier provide a high accuracy of ±1% (max) at 25°C. It is available in the DFN package.

Applications

- Smartphones, Tablets
- IP Cameras
- RF, PLL, VCO and Clock power supply
- Portable medical equipment

Typical Application

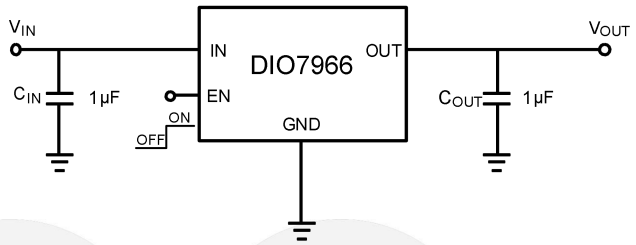


Figure 1. Typical Application

Ordering Information

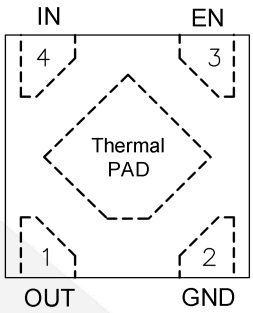
Order Part Number	Top Marking	Description		T_A	Package	
DIO7966AaaEN4	YW1X	Active Discharge	Green	-40 to +125°C	DFN1*1-4	Tape & Reel,10000
DIO7966BaaEN4	YW9X	Nonactive Discharge	Green	-40 to +125°C	DFN1*1-4	Tape & Reel,10000

Output Voltage Options								
Option Code "**aa**"	**10**	**12**	**15**	**18**	**25**	**28**	**30**	**33**
Voltage	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	2.8 V	3 V	3.3 V

Marking Definition	
YW1X	Y: year code; W: week code; 6: Product code;
YW9X	Y: year code; W: week code; 8: Product code;

Voltage code								
Option Code "X"	E	F	G	H	J	K	L	M
Voltage	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	2.8 V	3 V	3.3 V

Pin Assignments



DFN1*1-4

Figure 2. Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
EN	Enable Pin. This pin has an internal pull-down resistor. A logic low reduces the supply current to less than 1 μA. Connect to logic “High” for normal operation.
GND	Power Supply Ground.
IN	Input voltage supply pin
Thermal PAD	No connection

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage	-0.3 to 6	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3, max.6	V
V_{EN}	EN input voltage	-0.3 to 6	V
t_{SC}	Output short circuit duration	unlimited	s
$T_{J(MAX)}$	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C
$R_{\theta JA}$	Thermal resistance, junction−to−Air	198.1	°C/W
ESD	Human body model (HBM)	4000	V
	Charged device model (CDM)	2000	

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltage	1.65 to 5.5	V
T_A	Operating Free-Air Temperature	-40 to 125	°C

Electrical Characteristics

-40°C≤ T_J ≤125°C; V_{IN} = $V_{OUT(NOM)}$ + 1 V; I_{OUT} = 1 mA, C_{IN}=C_{OUT}=1 μF, unless otherwise noted. V_{EN} = 1.0 V. Typical values are at T_J = 25°C

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IN}	Operating input voltage			1.65		5.5	V
V_{OUT}	Output voltage accuracy	V_{IN} = $V_{OUT(NOM)}$ + 1 V I_{OUT} = 1mA, T_J = 25°C	V_{OUT}< 2 V	-20		+20	mV
			V_{OUT}≥ 2 V	-1		+1	%
$Line_{Reg}$	Line regulation	$V_{OUT(NOM)}$ +1 V < V_{IN} ≤ 5.5 V, T_J = 25°C				6	mV
$Load_{Reg}$	Load regulation	I_{OUT} = 1 mA to 250 mA			2		mV
V_{DO}	Dropout voltage	T_J = -40°C to 85 °C I_{OUT} = 250 mA	$V_{OUT(NOM)}$ = 3.3 V			100	mV
I_{CL}	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$		450	700		mA
I_{SC}	Short circuit current	V_{OUT}=0 V			180		mA
I_Q	Quiescent current	I_{OUT}=0 mA,T_J = 25°C			18	25	μA
I_{DIS}	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 4.8 V, T_J = 25°C			0.01	1	μA
V_{ENH}	EN pin threshold voltage	EN Input Voltage “H”		1			V
V_{ENL}		EN Input Voltage “L”				0.4	V
I_{EN}	EN pull down current	V_{EN} = 4.8 V,T_J = 25°C			0.2	0.5	μA
t_{ON}	Turn on time	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$			250		μs
PSRR	Power supply rejection ratio	I_{OUT} = 10 mA	f = 100 Hz		91		dB
			f = 1 kHz		95		
			f = 10 kHz		75		
			f = 100 kHz		55		
			f = 1 MHz		56		
V_N	Output voltage noise	f =10 Hz to 100 kHz	I_{OUT} = 1 mA		14		$μV_{RMS}$
			I_{OUT} = 250 mA		10		
T_{SDH}	Thermal shutdown threshold	Temperature rising			160		°C
T_{SDL}		Temperature falling			140		°C
R_{DIS}	Active output discharge resistance	V_{EN} < 0.4 V, Version A only			100		Ω
$Tran_{LINE}$	Line transient	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 μs, I_{OUT} = 1 mA		-1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 μs, I_{OUT} = 1 mA				+1	

$Tran_{LOAD}$	Load transient	I_{OUT} = 1mA to 250 mA in 10 μs	-40			mV
		I_{OUT} = 250 mA to 1 mA in 10 μs			+40	mV

Block Diagram

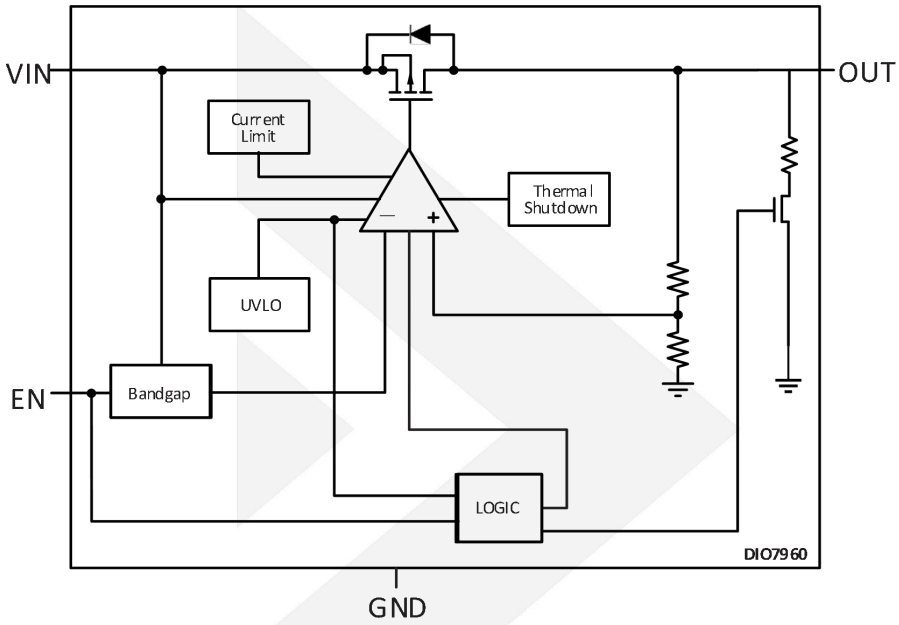


Figure 3. Block Diagram

Detailed Description

Overview

The DIO7966 series of LDO linear regulators are ultra-high PSRR and low noise devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provide overall 1% accuracy. Low output noise, very high PSRR, and low dropout voltage make this device ideal for most battery-operated handheld equipment. The DIO7966 is fully protected in case of current overload, output s d overheating.

Input Capacitor Selection (C_{IN})

The DIO7966 is specifically designed to work with a standard ceramic input capacitor. An input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used because of its minimal variation in the value and equivalent series resistance (ESR) over temperature. The value of the input capacitor should be 1μF or larger to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Capacitor Selection (C_{OUT})

The DIO7966 requires an output capacitance, and the value of the input capacitor should be 1μF or larger for stability. Use X5R- and X7R-type ceramic capacitors because of its minimal variation in value and equivalent series resistance (ESR) over temperature.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperatures.

Enable Operation

The DIO7966 uses the EN pin to enable/disable its device and discharge function (just for DIO7966). If the EN pin voltage is pulled below 0.4 V the device is guaranteed to be disable. The active discharge transistor at the devices with active discharge feature is activated and the output voltage V_{OUT} is pulled to GND through an internal circuitry with effective resistance about 100ohms.

If the EN pin voltage is higher than 1.0 V the device is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is available at output pin. In case of the enable function is not required, the EN pin should be connected directly to the input pin.

Output Current Limit

The DIO7966 internal current limit helps to protect the regulator during fault conditions. Output Current is internally limited within the IC to a typical 700 mA. During the current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until the thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between the current limit and thermal shutdown.

The PMOS pass element in the DIO7966 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Thermal Shutdown

When the chip temperature exceeds the Thermal Shutdown point (T_{SD}=160°C typical) the device goes to a disabled state and the output voltage is not delivered until the die temperature decrease to 140°C. The Thermal Shutdown feature protects from a catastrophic device failure at accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Dropout Voltage

The DIO7966 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$) of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the DIO7966 device can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}}$$

The power dissipated by the DIO7966 device for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \bullet I_{GND} + I_{OUT}(V_{IN} - V_{OUT})$$

Reverse Current

Reverse current flows through the body diode on the pass element instead of the normal conducting channel in the case that V_{OUT} > V_{IN}. Excessive reverse current can damage this device, so the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The DIO7966 features a very high Power Supply Rejection ratio to meet the requirements of RF and analog circuits. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

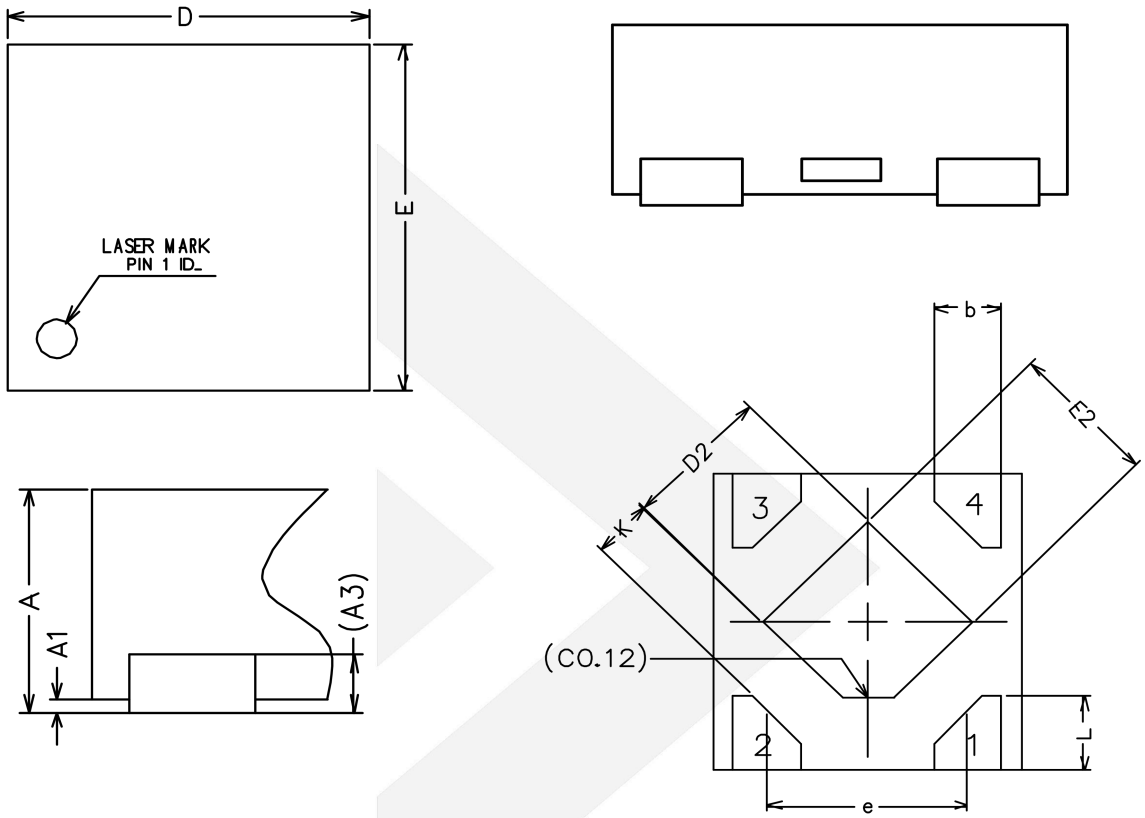
Turn−On Time

The turn−on time is defined as the period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

An optimal layout can greatly improve transient performance, PSR, and noise. To obtain excellent performance and good regulation characteristics, place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. Place ground return connections to the input and output capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. Expose pad can be tied to the GND pin for better power dissipation and lower device temperature.

Physical Dimensions: DFN1*1-4



COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	**MIN**	**NOM**	**MAX**
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3		0.100 REF.	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e		0.65 BSC.	
K	0.15	-	-

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as cell phones, handheld products, laptops, medical equipment, and so on. Dioo's product families include analog signal processing and amplifying, LED drivers, and charger ICs. Go to http://www.dioo.com for a complete list of Dioo product families.

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