

ACM5618 17-V, 15-A, High Efficiency, Fully-integrated Synchronous Boost Converter

1. Features

- Wide input voltage and output voltage range
 - VIN : 2.7-V to 17-V
 - VOUT : 4.5-V to 17-V
- 8-mΩ Low-side power FET R_{DS(on)} and 12-mΩ High-side power FET R_{DS(on)}
- Low quiescent current and shutdown current
- High power capability and efficiency
 - 15-A maximum peak current limit
 - 91% efficiency at VIN = 3.6-V, VOUT = 12-V and IOU_T = 2-A
 - 96% efficiency at VIN = 7.2-V, VOUT = 16-V and IOU_T = 3-A
- PFM mode in light load condition
- Programmable soft-start
- Programmable switching frequency between 300-kHz to 1.2-MHz
- Full protection
 - Programmable current limit threshold
 - Cycle by cycle current limit
 - Overvoltage protection at 17.2-V
 - Thermal shutdown
- 3.5-mm × 3.0-mm Flip-chip QFN package

2. Applications

- Bluetooth Speaker
- E-cigarette
- Quick charge power bank

3. General Description

ACM5618 is a fully integrated, high efficiency boost converter. The low power FET ON-resistance, 8-mΩ for low side and 12-mΩ for high side provides high efficiency and good thermal performance. ACM5618 has a wide input voltage range of 2.7-V to 17-V and a wide output voltage range of 4.5-V to 17-V, which makes it very suitable for single or two-series Li⁺ battery applications.

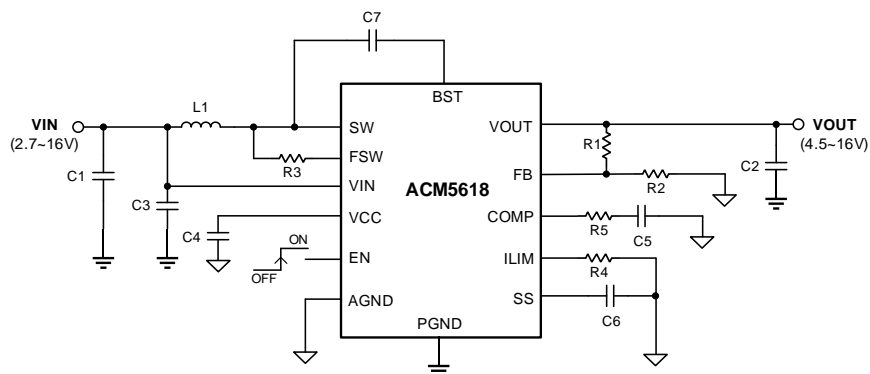
ACM5618 employs adaptive constant off-time peak current control mode to regulate the output voltage and ensure fast transient response. ACM5618 operates in the pulse width modulation (PWM) mode in moderate and heavy load condition. As the load current decreasing, it smoothly switches to pulse frequency modulation (PFM) mode to keep high efficiency operation. ACM5618 provides accurate regulation over wide load and V_{IN} range and keeps low output ripple.

ACM5618 provides 17.2-V output overvoltage protection, cycle-by-cycle current limit protection and thermal shutdown protection.

ACM5618 is available in a 3.5-mm × 3.0-mm QFN package.

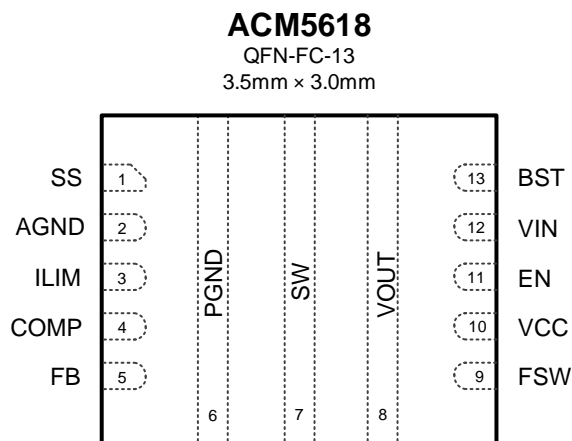
Device Information

Part number	Package	Body size (NOM)
ACM5618	QFN-FC-13	3.5 mm × 3.0 mm



Typical Application Circuit

4. Pin Configuration and Function Descriptions



(Top View)

Pin No.	Name	I/O Type	Description
1	SS	O	Soft-start programming pin. An external capacitor sets the ramp rate of the reference voltage of the internal error amplifier during soft start.
2	AGND	-	Analog signal ground of the IC. Connect the AGND to PGND via a single point on the printed circuit board.
3	ILIM	I	Programming the switching peak current limit by a resistor between this pin and AGND.
4	COMP	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and AGND.
5	FB	I	Output voltage feedback, a resistor divider connecting to this pin sets the output voltage.
6	PGND	-	Power ground.
7	SW	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power FET and the source of the internal high-side power FET.
8	VOUT	PWR	Boost converter output
9	FSW	I	The switching frequency is programmed by a resistor between this pin and the AGND. This pin can be left floating and the switching frequency will be set as default value.
10	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 1- μ F is required between this pin and ground.
11	EN	I	Enable logic input. Logic high level enables the device and low level shut down the device.
12	VIN	I	IC power supply input.
13	BST	O	Power supply for high-side FET gate driver. A capacitor must be connected between this pin and the SW pin.

5. Specifications

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	BST	-0.3	SW + 6	V
Voltage	VIN, VOUT, SW	-0.3	20	V
Voltage	ILIM, FB	-0.3	3.6	V
Voltage	Other pins	-0.3	6	V
T _A	Ambient operating temperature	-40	85	°C
T _{stg}	Storage temperature	-40	125	°C

- (1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.7		17	V
V _{OUT}	Output voltage range	4.5		17	V
L	Inductance (effective value)	0.47	2.2	10	μH
C _{IN}	Total input capacitance (effective value)	10			μF
C _{OUT}	Total output capacitance (effective value)	10	47	1000	μF
T _J	Junction Operating Temperature	-40		150	°C
T _A	Ambient Operating Temperature	-40		85	°C

5.4 Thermal Information

THERMAL METRIC		ACM5618 QFN-FC 13 PINS		UNIT
		JEDEC STANDARD 4-LAYER PCB	EVM 4-LAYER PCB	
θ _{JA}	Junction-to-ambient thermal resistance	60.2	TBC	°C/W
θ _{JT}	Junction-to-case (top) thermal resistance	28.6	N/A	°C/W
ψ _{JT}	Junction-to-top characterization parameter	14.5	N/A	°C/W

5.5 Electrical Characteristics

Free-are room temperature 25°C, test conditions is $V_{IN} = 3.7V$, $V_{OUT} = 12V$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Power Supply						
V_{IN}	Input voltage range	2.7		17	V	
V_{IN_UVLO}	V_{IN} Undervoltage lockout (UVLO) threshold	V_{IN} Falling	2.2	2.4	V	
V_{IN_HYS}	V_{IN} UVLO hysteresis		0.2		V	
V_{CC_UVLO}	V_{CC} UVLO threshold	V_{CC} Falling		2.1	V	
I_{Q_IN}	Quiescent current into V_{IN} pin	IC enabled, $V_{EN} = 2V$, no switching, $V_{OUT} > 1.05 V_{IN}$			10 μA	
I_{Q_OUT}	Quiescent current into V_{OUT} pin	IC enabled, $V_{EN} = 2V$, no switching, $V_{OUT} > 1.05 V_{IN}$			200 μA	
I_{SD}	Shutdown current	IC enabled, $V_{EN} = 0V$, no load, no feedback resistors. Measure the current into V_{IN} pin.		1	3 μA	
V_{CC}	Internal regulator output voltage	$I_{VCC} = 5mA$, $V_{IN} = 8V$		5	V	
EN INPUT						
V_{ENH}	EN high threshold voltage	$V_{CC} = 5V$			1.2 V	
V_{ENL}	EN low threshold voltage	$V_{CC} = 5V$	0.4		V	
R_{EN}	EN internal pull-down resistance	$V_{CC} = 5V$		800	k Ω	
OUTPUT						
V_{OUT}	Output voltage range		4.5		17 V	
I_{LKG_FB}	FB pin leakage current	$V_{FB} = 1V$			100 nA	
I_{SS}	Soft-start charging current			5	μA	
Power MOSFET						
$R_{DS(ON)}$	Low-side MOSFET ON-resistance (including lead frame metallization)	$V_{CC} = 5V$		8	m Ω	
	High-side MOSFET ON-resistance (including lead frame metallization)	$V_{CC} = 5V$		12		
ERROR AMPLIFIER						
V_{REF}	Internal reference voltage on FB pin	Operating in PWM	0.985	1	1.015	V
		Operating in PFM		1.01		
I_{SOURCE}	Comp pin maximum sourcing current	$V_{FB} = V_{REF} - 200mV$, $V_{COMP} = 1.5V$		20	μA	
I_{SINK}	Comp pin maximum sinking current	$V_{FB} = V_{REF} + 200mV$, $V_{COMP} = 1.5V$		20	μA	
V_{COMPH}	COMP clamp voltage high	$V_{FB} = V_{REF} - 200mV$		2	V	
V_{COMPL}	COMP clamp voltage low	$V_{FB} = V_{REF} + 200mV$		1	V	
G_{EA}	Error amplifier trans-conductance			175	$\mu A/V$	
G_{PS}	Power stage trans-conductance ($\Delta I_{L_PEAK} / \Delta V_{COMP}$)			13.5	A/V	
SWITCHING TIMING						
F_{SW}	Switching frequency	$R_{FREQ} = 100 k\Omega$		550	kHz	
T_{ON_MIN}	Low side Power FET minimum ON time	$R_{FREQ} = 100 k\Omega$		70	ns	
PROTECTION						
I_{LIM}	Peak current limit on power FET	$R_{LIM} = 110 k\Omega$	13.5	15	A	
V_{OVP_THES}	V_{OUT} over-voltage protection threshold	V_{OUT} rising		17.5	V	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OVP_HYS}	V _{OUT} over-voltage protection auto-recovery hysteresis	V _{OUT} falling below V _{OVP_THES}		0.3		V

Free-are room temperature 25°C, test conditions is V_{IN} = 3.7V, V_{OUT} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T _{OTSD}	Over-temperature shutdown threshold	T _J rising		150		°C
T _{OTSD_HYS}	Over-temperature shutdown auto-recovery hysteresis	T _J falling below T _{OTSD}		20		°C

5.6 Typical Characteristics

Free-air room temperature 25°C (unless otherwise noted.)

6. Detailed Description

6.1 Overview

The ACM5618 is a fully-integrated synchronous boost converter with an 8-m Ω power switch and a 12-m Ω rectifier switch to deliver high power from a single-cell or two-cell Lithium batteries. The input voltage range is 2.7-V to 17-V and the output range is 4.5-V to 17-V.

The ACM5618 employs adaptive constant off-time peak current control mode to regulate the output voltage. In moderate-to-heavy load condition, the ACM5618 works in the quasi-constant frequency pulse width modulation (PWM) mode. The switching frequency in PWM mode is adjustable ranging from 200-kHz to 2.2-MHz by an external resistor. In light load condition, the ACM5618 works in pulse frequency modulation (PFM) mode, which skips the unnecessary pulses and keeps high efficiency. The ACM5618 implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The switch peak current limit is programmable by an external resistor. The ACM5618 uses external loop compensation, which provides flexibility to use different inductors and output capacitors. The adaptive off-time peak current control scheme gives excellent line/load transient response with minimal output capacitance.

6.2 Functional Block Diagram

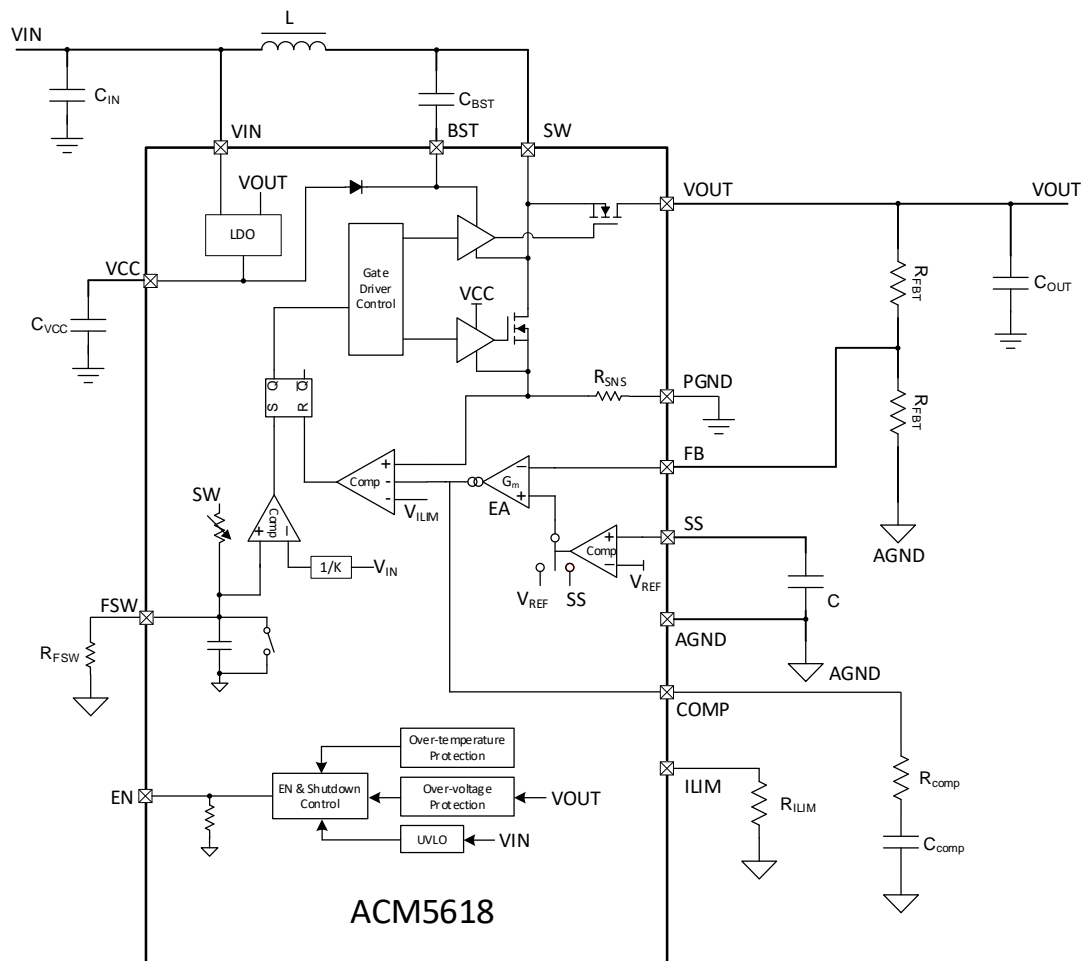


Figure 6-1. Functional Block Diagram

6.3 Detail Feature Description

6.3.1 Enable and Start-up

The ACM5618 has an EN pin to enable or disable the device. Pulling the EN pin to logic high, the device is enabled and the start-up sequence is initialized. Pulling the EN pin to logic low, the device is disabled. The switching is stopped and the output starts to decay.

During the start-up, the ACM5618 supports adjustable soft-start function to avoid in-rush current. The device sources a constant current of 5- μ A typically out of the SS pin, charging the external capacitor C_{SS} and building a ramping up voltage. This voltage is fed into the positive input of the internal error amplifier until it goes higher than the internal reference voltage, which is 1.204-V typically. The capacitance connected to the SS pin determines how fast the VOUT ramps up. Equation 6-1 gives the calculation of the soft-start time,

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}} \quad (\text{Eq.6-1})$$

where,

- t_{SS} is the soft-start time
- V_{REF} is the internal reference voltage, which is 1.204-V typically
- C_{SS} is the external capacitance connected to SS pin
- I_{SS} is the soft-start charging current, which is 5-uA typically

A 47-nF capacitor could cover most application circumstances. As the SS voltage ramps up during the soft-start phase, once it exceeds the internal reference voltage, the positive input of the internal error amplifier is taken over by the internal reference voltage, indicating the soft-start phase is completed. When the EN pin is pulled low, the C_{SS} is discharged to GND.

6.3.2 Undervoltage Lockout

The UVLO feature protects the device from the possible malfunction when operating at low input voltage, which could result from an excessively discharged battery or a brownout event. The ACM5618 monitors both the VIN and VCC for the UVLO. When the VIN falling below the UVLO threshold V_{IN_UVLO} , which is typically 2.4-V, the ACM5618 stops switching. The ACM5618 will not recover to operating until VCC and VIN get higher than ($V_{IN_UVLO} + 200\text{mV}$). When the VCC falling below the UVLO threshold V_{CC_UVLO} , which is typically 2.1-V, the ACM5618 stops switching.

6.3.3 Adjustable Switching Frequency

The ACM5618 provide four options of switching frequency. Low switching frequency provides higher efficiency but may not have good transient performance. It should also be noted that higher switching frequency results in lower inductor current ripple, which may be the bottle-neck in some high VOUT/VIN ratio applications. ACM5618 employs an external resistor R_{FSW} connected between FSW pin and GND to set the switching frequency. If the FSW pin is left floating, the switching frequency will be set to 550-kHz as default. Table 6-1 shows the detail configurations.

Table 6-1. Switching Frequency Options

R_{FSW}	Switching Frequency
51 k Ω	300 kHz
100 k Ω	550 kHz
200 k Ω	800 kHz
390 k Ω	1 MHz

6.3.4 Adjustable Peak Current Limit

To avoid excessive peak current on power switch, an internal cycle-by-cycle current limit is implemented on ACM5618. In battery powered systems, the adjustable peak current limit could also be used to limit the battery discharge current to avoid brownout events. The low-side switch will be turned off immediately once the current arrives the current limit. The peak switch current limit can be programmed by an external resistor connected between ILIM pin and GND. Use Equation 6-2 to calculate the resistor value for a selected current limit,

$$I_{LIM} = \frac{1650000}{R_{ILIM}} \quad (\text{E.q. 6-2})$$

where,

- R_{ILIM} is the resistance connected between ILIM pin and GND
- I_{LIM} is the switch peak current limit

6.3.5 Overvoltage Protection

The ACM5618 stops switching immediately when the VOUT exceeds the output overvoltage protection threshold V_{OVP_THES} , which is 17.2-V typically. The normal operation will not recover until the VOUT drops a hysteresis value lower than the V_{OVP_THES} , which is typically 500-mV. The over voltage protection is non-latched and the device could automatically recover after the fault condition removed.

6.3.6 Over Temperature Protection

An over-temperature protection is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown is triggered when the junction temperature exceeds 150°C. The normal operation will not recover until the junction temperature falls below 130°C typically. The over temperature protection is non-latched and the device could automatically recover after the fault condition removed.

6.4 Device Function Modes

6.4.1 Operation

6.4.1.1 PWM Mode

The synchronous boost converter ACM5618 employs adaptive-off time control scheme. It operates at a quasi-constant frequency pulse width modulation in moderate-to-heavy load condition. The ACM5618 integrates a dedicate circuit to predict the low-side off-time based on the VIN and VOUT voltage. At the beginning of each period, the low-side switch is turned on. The inductor current starts to ramp up. The low-side current is sensed and compared to the output of the error amplifier. Once the comparator output toggled, the low-side switch is turned off and the inductor current starts to ramp down. After a dead-time duration, the high-side switch is turned on, taking over the inductor current from its body diode. The high-side switch keeps ON status until the time-out event from the off-time prediction circuit. Then the low-side switch turns on after a dead time duration and a new period starts.

6.4.1.2 PFM Mode

At light load conditions, the ACM5618 automatically enters the pulse frequency modulation (PFM) mode. As the loading current goes down, the current flowing through the high-side switch decreases to zero during the off time. The high side switch is turned

off at zero-crossing point. The status is kept until next period starts and the low side switch turned on. If the loading current continuously decrease and reaches a threshold of $1/12 I_{LIM}$, the output of the error amplifier is clamped at this value. If the loading current is still lower than the average current ACM5618 delivers, the output voltage increases above the nominal setting output voltage. The ACM5618 extends the off-time to decrease the energy delivered to the output and regulate the output voltage to 0.8% higher than the nominal setting.

7 Application and Implementation

7.1 Application Information

The ACM5618 is capable to support up to 17-V output voltage and up to 15-A switch current, delivering more than 50-W output power. It is quite suitable for applications powered by single-cell and 2-s cell Li⁺ battery. The ACM5618 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate-to-heavy load condition. In light load condition, the ACM5618 operates in PFM mode, keeping high efficiency in entire loading range. The ACM5618 employs the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The ACM5618 works well with various inductor and output capacitor combinations by external loop compensation. It also supports four switching frequency options and programmable current limit.

7.2 Typical Application

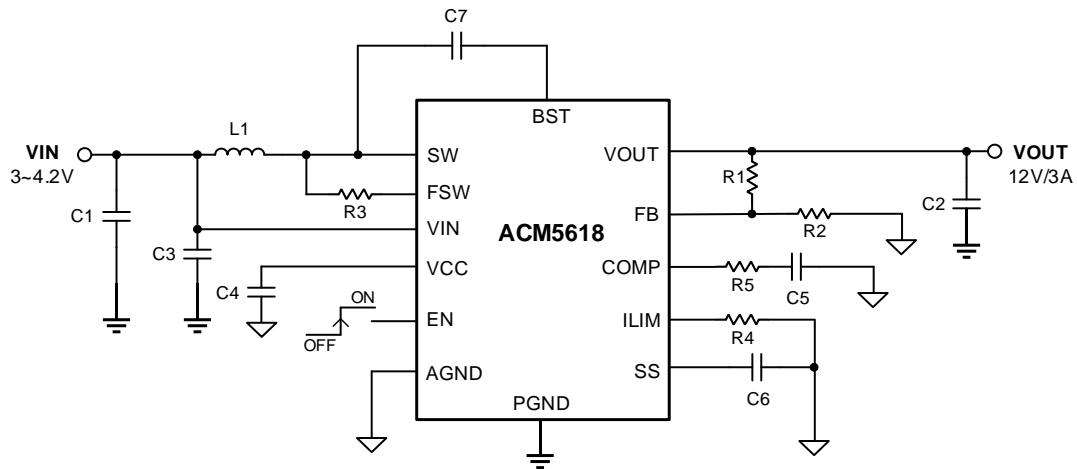


Figure 7-1 ACM5618 3.7V to 12V/3.5A Application circuit

7.2.1 Design Requirements

Table 7-1. Design Parameters

Design Parameters	Recommended Values
Input voltage range	3.4~4.2V
Output voltage	12V
Output voltage ripple (V_{pp})	100mV
Switching Frequency	550kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Switching Frequency Setting

The ACM5618 supports 4 switching frequency options. The switching frequency is set by the resistance connected between FSW pin and GND. In this example, a 100-k Ω resistor is connected to set the 550-kHz F_{sw} to take a balance among efficiency, thermal and line/load transient performance.

7.2.2.2 Peak Current Limit Setting

7.2.2.3 Output Voltage Setting

For ACM5618, the output voltage is set by an external resistor divider (R1, R2 in Figure 7-1). Typically, a minimum current of 30- μ A flowing through the feedback divider gives good accuracy and noise rejection, thus a standard 33-k Ω resistor is selected for the bottom resistor in the divider. Equation 7-1 gives the output voltage setting calculation,

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (\text{Eq. 7-1})$$

7.2.2.4 Inductor Selection

As the inductor has significant impact on the steady state operation of the power supply, transient performance, loop stability

and efficiency, the inductor is the most important component in switching power regulator design. Four main specifications for the inductor selection are the inductance, the DC resistance, the saturation current and the rated DC current.

The ACM5618 is designed to work with $0.47\text{-}\mu\text{H}\sim 10\text{-}\mu\text{H}$ inductance. A $0.47\text{-}\mu\text{H}$ inductor is typically available in a smaller or lower-profile package with higher saturation current and rated DC current capability, while a $10\text{-}\mu\text{H}$ inductor produces lower inductor current ripple. If the output current is limited by the peak current limit of the IC, using a $10\text{-}\mu\text{H}$ inductor can maximize the output current capability of the boost converter.

Usually, the inductance can have $\pm 20\%$ or even $\pm 30\%$ tolerance with no current bias. When the inductor current approaches saturation level, the inductance can decrease 20% to 30% from nominal value, depending on how the inductor vendor defines saturation current. When selecting an inductor, make sure the saturation current is higher than its peak current during the operation and the rated DC current is higher than the RMS value of the inductor current in normal operation.

Follow Equation 7-3 and Equation 7-4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, it is recommended to use the minimum switching frequency, the inductor value with 30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 7-2.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (\text{E.q. 7-2})$$

where,

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the efficiency of the boost circuit

Inductor current ripple is given by Equation 7-3,

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_{SW}} \quad (\text{E.q. 7-3})$$

where,

- I_{PP} is the peak-to-peak current ripple on the inductor
- L is the inductor value
- F_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Furthermore, the peak current, I_{L_PEAK} is given by,

$$I_{L_peak} = I_{DC} + \frac{I_{PP}}{2} \quad (\text{E.q. 7-4})$$

The current limit of the ACM5618 should be set higher than the peak current I_{L_peak} . The saturation current of the inductor should be higher than the current limit setting.

Boost converter efficiency mainly depends on the resistance of the current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The ACM5618 has optimized the internal switch resistance. However, the overall efficiency is still affected significantly by the DC resistance (DCR) of the inductor and the inductor core loss. The core loss is related to the magnetic material of the core. Different inductors could have quite different core loss performance. Larger inductor current ripple generates higher DCR conduction losses and higher core loss. In most cases, the core loss information is not shown on the inductor datasheet. If needed, consult the inductor vendor for detailed information. Generally, ACME would recommend an inductor with lower DCR. However, there is always tradeoff among the inductance, DCR and its footprint.

Table 7-2 lists several recommended inductors for the ACM5618.

Table 7-2 Inductor Recommendations

Part Number	L (μH)	DCR Max (mΩ)	Saturation Current/ Heat Rating Current (A)	Size (L×W×H mm)	Manufacturer

7.2.2.5 Input Capacitor Selection

For battery powered systems, to smooth the battery discharge current, large input capacitance is recommended, for example, a 220-μF electrolytic capacitor. For other none battery powered systems, usually a 22-μF capacitance is good enough. As a rule of thumb, a sufficient input capacitance should make the input voltage ripple lower than 100-mV.

The VIN pin is the power supply for the ACM5618, a 0.1-μF low-ESR ceramic bypass capacitor is recommended and should be placed as close as possible to the VIN pin. The VCC is the output of the internal LDO. Connect a 1-μF ceramic capacitor between VCC pin and AGND is recommended for normal operation of the internal LDO.

It should also be noted that the effective capacitance of the ceramic capacitors may decrease as the DC voltage across the capacitor increase, which is also known as DC bias effect. Make sure there is enough effective capacitance for all the capacitors mentioned above.

7.2.2.6 Output Capacitor Selection

For the applications where lower output voltage ripple is the priority, ACME recommends low-ESR output capacitors like MLCC. Typically, three 22-μF ceramic output capacitors works well for most applications. Take care when evaluating the derating of a capacitor under DC bias. The bias can significantly reduce effective capacitance of the MLCC. Ceramic capacitors may lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating is necessary to ensure adequate effective capacitance.

For the applications where good load transient performance is required, a larger output capacitance is recommended. Electrolytic capacitors and MLCC can be put in parallel to balance the output ripple and stable output during load transient events. However, in some applications where the boost output voltage dynamically changes, for example, the Class-H application with ACME audio amplifiers, large output capacitance may increase the burden of the input current peak, as it takes extra current to charge the output capacitance up and raise the output voltage.

Use the Equation 7-5 to Equation 7-7 to estimate the output capacitance according to the output ripple requirement.

$$V_{ripple_cap} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times F_{SW} \times C_{OUT}} \quad (\text{E.q. 7-5})$$

$$V_{ripple_res} = I_{L_peak} \times R_{C_ESR} \quad (\text{E.q. 7-6})$$

$$V_{ripple} = \sqrt{V_{ripple_cap}^2 + V_{ripple_res}^2} \quad (\text{E.q. 7-7})$$

where,

- V_{ripple_cap} is output voltage ripple caused by charging and discharging of the output capacitor
- V_{ripple_res} is output voltage ripple caused by ESR of the output capacitor
- V_{IN_MIN} is the minimum input voltage of boost converter
- V_{OUT} is the output voltage

- I_{OUT} is the output current
- I_{L_peak} is the peak current of the inductor
- F_{SW} is the converter switching frequency
- R_{C_ESR} is the ESR of the output capacitors

7.2.2.7 Loop Stability

The ACM5618 requires external loop compensation, which usually formed by a serial R-C network connected to COMP pin. The COMP pin is the output of the internal error amplifier. A capacitor can also be added in parallel with the serial R-C to provide extra high frequency rolling. The detail calculation steps for loop compensation design will be discussed in the following section.

The small-signal model transfer function of power stage is given by Equation 7-8,

$$G_{PS}(S) = \frac{R_O \times (1-D)}{2 \times R_{SNS}} \times \frac{(1 - \frac{s}{2\pi \times f_{RHPZ}})(1 + \frac{s}{2\pi \times f_{ESRZ}})}{(1 + \frac{s}{2\pi \times f_p})} \quad (\text{E.q. 7-8})$$

where,

- D is the switching duty cycle
- R_O is the output load resistance
- R_{SNS} is the equivalent internal current sense resistor, which is 0.0075 Ω

The f_{RHPZ} is the right half plane zero, given by

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad (\text{E.q. 7-9})$$

where,

- L is the inductance

The f_{ESRZ} is the zero introduced by the equivalent series resistance of the output capacitor, given by

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (\text{E.q. 7-10})$$

The f_p is the dominant load pole, given by,

$$f_p = \frac{1}{2\pi \times R_O \times C_{OUT}} \quad (\text{E.q. 7-11})$$

The COMP pin is connected to the output of the internal error amplifier, which is a trans-conductance amplifier. The overall transfer function of the feedback and compensation blocks is given by,

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1 + \frac{s}{2\pi \times f_{z_COMP}})}{(1 + \frac{s}{2\pi \times f_{p_COMP}})(1 + \frac{s}{2\pi \times f_{p_ROLL}})} \quad (\text{E.q. 7-12})$$

where

- G_{EA} is the transconductance of the amplifier
- R_{EA} is the output resistance of the amplifier
- V_{REF} is the reference voltage on the FB pin
- V_{OUT} is the output voltage

The f_{p_COMP} , f_{p_ROLL} are the poles introduced by the compensation network, given by

$$f_{p_COMP} = \frac{1}{2\pi \times R_{EA} \times C_{COMP}} \quad (\text{E.q. 7-13})$$

where

- R_{EA} is the equivalent output resistance of the error amplifier
- C_{COMP} is the capacitor in the R-C compensation network

$$f_{p_ROLL} = \frac{1}{2\pi \times R_{COMP} \times C_{ROLL}} \quad (\text{E.q. 7-14})$$

where

- R_{COMP} is the resistor in the R-C compensation network
- C_{ROLL} is the optional capacitor in parallel with the R-C compensation network

The f_{z_COMP} is the zero introduced by the compensation network, given by,

$$f_{z_COMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (\text{E.q. 7-15})$$

8. Layout

9. Package Dimensions

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM5618	QFN-FC-13 Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM5618