DIO4483

USB Type-C Analog Audio Switch with Protection Function + Comparator

Features

- Power Supply Voltage Range: 2.7V to 5.5V
- USB2.0 High Speed Switch:
  - −3dB bandwidth: 950MHz
  - 4.6Ω R_{ON} Typical
- Audio Switch
  - Negative Rail Capability: −3.6V to 3.6V
  - THD+N=-110dB, 1V_{RMS}, f=20Hz~20kHz, 32Ω Load
  - −3dB bandwidth: 800MHz
  - 1.2Ω R_{ON} Typical
- UART High Speed Switch:
  - −3dB bandwidth: 800MHz
  - 15.1Ω R_{ON} Typical
- High Voltage Protection
  - +20V DC Tolerance on USB Type-C Pins
  - +25V Surge Capable on USB Type-C Pins
  - ±2kV HBM ESD
- Over Voltage Protection:
  - DP/R, DN/L, SBU1/SUB2/GSBU1/GSBU2 V_{TH} = 4.4V(default), 4.4V~5.0V configurable
- Support OMTP, CTIA and 3-Pole audio jack Pinout
- Built-in comparator, normally active
- 25-Ball WLCSP Package (2.24mm*2.28mm)

Applications

- Mobile Phone
- Tablet
- Notebook PC
- Media Player

Descriptions

DIO4483 is a high performance USB Type−C analog switch used in portable multimedia devices, which supports analog audio headsets. DIO4483 can detect OMTP, CTIA or 3-Pole headset and configure pinout automatically. DIO4483 shares common Type−C pins to pass USB2.0 signal and analog audio signal, sideband use wires and analog microphone signal. DIO4483 also supports high voltage and surge on SBUx pins and USB pins on USB Type−C receptacle side.

The internal ultra low-power comparator with a typical power supply current of 0.3μA. It has the best-in-class power supply current versus propagation delay performance. Featuring a push-pull output stage, the comparator allows for operation with absolute minimum power consumption when driving any capacitive or resistive load.

Block Diagram

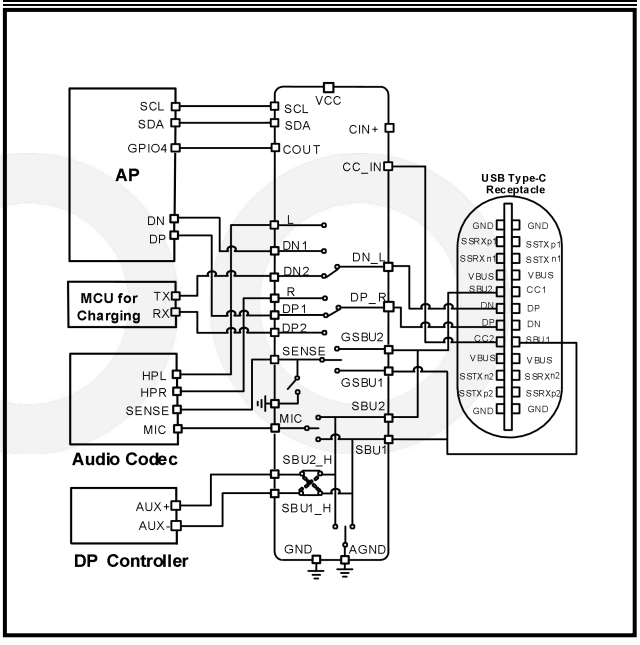
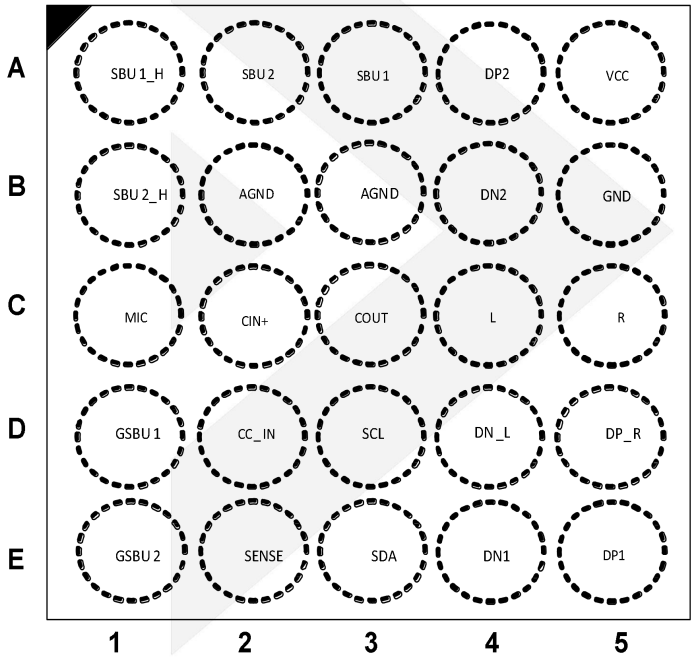


Figure 1. Application Block Diagram

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO4483WL25	D4HC	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000

Pin Assignment



WLCSP-25

Figure 2. Top View

Pin Descriptions

Pin	Name	Description
A5	VCC	Power Supply (2.7 to 5.5V)
B5	GND	Chip ground
D5	DP_R	USB/Audio Common Pin
D4	DN_L	USB/Audio Common Pin
E5	DP1	USB Data1 (Differential +)
E4	DN1	USB Data1 (Differential –)
C5	R	Audio – Right Channel
C4	L	Audio – Left Channel
A3	SBU1	Sideband use wire 1
A2	SBU2	Sideband use wire 2
C1	MIC	Microphone signal
B2	AGND	Audio signal ground
B3	AGND	Audio signal ground
E2	SENSE	Audio ground reference output
C3	COUT	Open Drain Comparator OUT.
D2	CC_IN	Audio accessory attachment detection input
D1	GSBU1	Audio sense path 1 to headset jack GND
E1	GSBU2	Audio sense path 2 to headset jack GND
C2	C1N+	Comparator IN+
D3	SCL	I^2C clock
E3	SDA	I^2C data
B1	SBU2_H	Host Side Sideband Use Wire 2
A1	SBU1_H	Host Side Sideband Use Wire 1
A4	DP2	USB Data2 (Differential +)
B4	DN2	USB Data2 (Differential –)

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage from VCC		−0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND		−0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND		−3.5	20	V
V_{SW_USB}	V_{DP1} to GND, V_{DN1} to GND		−0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		−3.6	6.5	V
V_{SW_UART}	V_{DP2} to GND, V_{DN2} to GND		−3.6	6.5	V
$V_{V\_SBUx/GSBUx}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND		−0.5	20	V
V_{VSBUx_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		−0.5	6.5	V
$V_{I/O}$	SENSE, MIC, to GND		−0.5	6.5	V
V_{CNTRL}	Control Input Voltage	SDA, SCL	−0.5	6.5	V
$V_{comparator}$	Comparator input and output	CIN+, COUT	−0.5	6.5	V
I_{SW_Audio}	Switch I/O Current, Audio Path		−250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path		−	100	mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2		−	50	mA
I_{SW_SBUx}	Switch I/O Current, SBUx to SBUx_H		−	50	mA
I_{SW_SENSE}	Switch I/O Current, SENSE to GSBU1 or GSBU2		−	100	mA
I_{SW_AGND}	Switch I/O Current, AGND to SBU1 or SBU2		−	500	mA
I_{IK}	DC Input Diode Current		−50	−	mA
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001	Connector side and power pins: VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN	8	−	kV
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001	Host side pins: the rest pins	4	−	kV
T_A	Absolute Maximum Operating Temperature		−40	85	°C
T_{STG}	Storage Temperature		−65	150	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER					
V_{CC}	Supply Voltage	2.7	–	5.5	V
USB SWITCH					
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0	–	3.6	V
AUDIO SWITCH					
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	−3.6	–	3.6	V
MIC SWITCH					
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0	–	3.6	V
SENSE SWITCH					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0	–	3.6	V
SBU TO SBUX_H SWITCH					
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0	–	3.6	V
CC_IN PIN					
V_{CC_IN}	$V_{CC\_IN,}$ to GND	0	–	5.5	V
CONTROL VOLTAGE (ENN/SDA/SCL)					
V_{IH}	Input Voltage High	0.825	–	V_{CC}	V
V_{IL}	Input Voltage Low	–	–	0.3	V
OPERATING TEMPERATURE					
T_A	Ambient Operating Temperature	−40	25	85	°C
Comparator					
Supply Voltage		2.7		5.5	V
Quiescent current	T_A=25°C	500 (Max)			nA
	T_A=–40°C to 125°C	1000 (Max)			nA

DC Electrical Characteristics

V_{CC}=2.7V to 5.5V, V_{CC}(Typ.)=3.3V, T_A=-40°C to 85°C, and T_A(Typ.)=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	V_{CC}: 4.2V		55		μA
		Audio switches on, MIC switch on and Audio GND switch on			53		μA
I_{CCZ}	Quiescent Current	04H'b7 = 0			4		μA
USB/AUDIO COMMON PINS: DP/R, DN_L							
I_{OZ}	Off Leakage Current of DP_R and DN_L	DN_L, DP_R = −3V to 3.6V	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OFF}	Power−Off Leakage Current of DP_R and DN_L	DN_L, DP_R = 0V to 3.6V	Power off	-3		3	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC}: 2.7V to 5.5V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP Hysteresis				0.24		V
AUDIO SWITCH							
I_{ON}	On Leakage Current of Audio Switch	DN_L, DP_R = −3V to 3V, DP, DN, R, L = Float	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OFF}	Power−Off Leakage Current of L and R	L, R = 0V to 3V; DP_R, DN_L = Float	Power off	-1		1	μA
R_{ON}	Switch On Resistance	I_{SW} = 100mA, V_{SW} = −3V to 3V	V_{CC}: 2.7V to 5.5V		1.2		Ω
R_{SHUNT}	Pull Down Resistor on R/L Pin when Audio Switch is Off	L= R = 3V		6	10	14	kΩ
USB SWITCH							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0V to 3.6V, DP, DN, R, L = Float	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V		-3		3	μA
I_{OFF}	Power−Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	Power off	-3		3	μA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8mA, V_{SW} = 0.4V	V_{CC}: 2.7V to 5.5V		4.6		Ω
UART SWITCH							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0V to 3.6V, DP, DN, R, L = Float	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V		-3		3	μA

I_{OFF}	Power−Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	Power off	-3		3	μA
R_{ON_UART}	UART Switch On Resistance	I_{SW} = 3mA, V_{SW} = 0.4V	V_{CC}: 2.7V to 5.5V		15.1		Ω
SENSE-AGND SWITCH							
R_{ON}	SENSE Switch On Resistance	I_{OUT} = 100mA, V_{SW} =1.0V	V_{CC}: 2.7V to 5.5V		5		Ω
SENSE SWITCH							
I_{ON}	Sense Path Leakage Current	GSBUx = 0V to 1V, SENSE is floating	V_{CC}: 2.7V to 5.5V	-2		2	μA
R_{ON}	SENSE Switch On Resistance	I_{OUT} = 100mA, V_{SW} =1.0V	V_{CC}: 2.7V to 5.5V		330		mΩ
I_{OZ}	Off Leakage Current of SENSE	Sense = 0V to 1.0V	V_{CC}: 2.7V to 5.5V	-2		2	μA
	Off Leakage Current of GSBUx	GSBUx = 1V to 3.6V		-3		3	μA
I_{OFF}	Power−Off Leakage Current of SENSE	Sense = 0V to 1.0V	V_{CC}: 2.7V to 5.5V	-2		2	μA
	Power−Off Leakage Current of GSBUx	GSBUx = 0V to 3.6V		-3		3	μA
V_{OV_TRIP}	Input OVP Lockout on GSBUx	Rising edge	V_{CC}: 2.7V to 5.5V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx				0.25		V
SBUX PINS							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0V to 3.6V	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OFF}	Power−Off Leakage Current Port SBUx	SBUx = 0V to 3.6V	Power off	-2		10	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC}: 2.7V to 5.5V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP Hysteresis				0.25		V
MIC SWITCH							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0V to 3.6V, MIC is floating	V_{CC}: 2.7V to 5.5V	-3		3	μA
I_{OZ}	Off Leakage Current of MIC	MIC = 0V to 3.6V		-1		1	μA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0V to 3.6V	Power off	-1		1	μA
R_{ON}	MIC Switch On Resistance	V_{SW} = 3.6V, Isw = 30mA	V_{CC}: 2.7V to 5.5V		3.1		Ω
SBUX_H SWITCH							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0V to 3.6V, SBUx_H is floating	V_{CC}: 2.7V to 5.5V	-3		3	μA

I_{OZ}	Off Leakage of SBUx_H	SBUx_H = 0V to 3.6V		-1		1	μA
I_{OFF}	Power Off Leakage Current of SBUx_H	SBUx_H = 0V to 3.6V	Power off	-1		1	μA
R_{ON}	SBUx_H Switch On Resistance	V_{SW} = 0V to 3.6V, Isw = 30mA	V_{CC}: 2.7V to 5.5V		2.8		Ω
AUDIO GROUND SWITCH: PIN: AGND TO SBUX							
R_{ON}	AGND Switch On Resistance	I_{SOURCE} = 100mA on SBUx	V_{CC}: 2.7V to 5.5V		66		mΩ
CC_IN PIN							
V_{TH_L}	Input Low Threshold		V_{CC}: 2.7V to 5.5V		1.2		V
V_{TH_H}	Input High Threshold				1.5		V
I_{IN}	Input Leakage of CC_IN	CC_IN = 0V to 5.5V				1.0	μA
SDS, SCL PINS							
V_{ILI2C}	Low−Level Input Voltage		V_{CC}: 2.7V to 5.5V			0.3	V
V_{IHI2C}	High−Level Input Voltage			0.825			V
I_{I2C}	Input Current of SDA and SCL Pins	SCL/SDA = 0V to 3.6V		-5		5	μA
V_{OLSDA}	Low−Level Output Voltage	I_{OL} = 2mA				0.3	V
I_{OLSDA}	Low−Level Output Current	V_{OLSDA} = 0.2V		10			mA
OVP							
V_{OV_TRIP}	Input OVP Lockout on receptacle side pin	Rising edge	V_{CC}: 2.7V to 5.5V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP Hysteresis of DP/R,DN/L,SBU_X, GSBUx on receptacle side pin				0.25		V

Comparator Electrical Characteristics

At T_A=25°C, V_{CC}=2.3V to 5V, C_L=15pF, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Offset Voltage						
V_{REF}	Reference Voltage	T_A=25°C to 65°C	218.5	225	231.5	mV
V_{HYS}	Hysteresis			20	30	mV
dV_{OS}/dT	Input offset voltage drift	T_A=–40°C to 125°C			±70	μV/°C
Input Voltage Range						
V_{CM}	Common-mode voltage range	T_A=–40°C to 125°C	- 0.1		V_{CC}+0.1	V
Input Bias Current						
I_B	Input bias current	T_A=25°C		30	100	pA
		T_A=–40°C to 125°C			20	nA
I_{OS}	Input offset current			8		pA
C_{LOAD}	Capacitive load drive			60		pF
Output Type		Open-Drain				

AC Electrical Characteristics

V_{CC}=2.7V to 5.5V, V_{CC} (Typ.) =3.3V, T_A=-40°C to 85°C, and T_A (Typ.) =25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min.	Typ.	Max.	Unit
AUDIO SWITCH							
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1V, R_L = 32Ω	V_{CVC}= 3.3V		40		μs
t_{rise}	Audio Switch Turn On Rising Time (Note 1)	DP_R = DN_L = 1V, R_L = 32Ω			75		μs
t_{OFF}	Audio Switch Turn Off Time	DP_R = DN_L = 1V, R_L = 32Ω			7		μs
X_{TALK}	Cross Talk (Adjacent)	f = 1kHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$			-90		dB
BW	−3dB Bandwidth	R_L = 50Ω			800		MHz
O_{IRR}	Off Isolation	f = 1kHz, R_L = 50Ω, C_L =0pF, V_{SW} = $1V_{RMS}$			-95		dB
THD+N	Total Harmonic Distortion + Noise Performance with A−weighting Filter	R_L = 600Ω, f = 20Hz~20kHz, V_{SW} = $2V_{RMS}$			-110		dB

		R_L= 32Ω, f = 20Hz~20kHz, V_{SW} = 1V_{RMS}			-110		dB
		R_L = 16Ω, f = 20Hz~20kHz, V_{SW} = 0.5V_{RMS}			-108		dB
USB SWITCH							
t_{ON}	USB Switch Turn−on Time	DP_R = DN_L =1.5V, R_L = 50Ω	V_{CC}= 3.3V		40		μs
t_{OFF}	USB Switch Turn −off Time	DP_R = DN_L =1.5V, R_L = 50Ω			6		μs
BW	−3dB Bandwidth	R_L = 50Ω			950		MHz
O_{IRR}	Off Isolation between DP, DN and Com- mon Node Pins	f = 1kHz, R_L = 50Ω, C_L =0pF, V_{SW} =1V_{RMS}			-100		dB
t_{OVP}	DP_R and DN_L pins OVP Response Time	Vsw = 3.5V to 5.5V			0.4		μs
UART SWITCH							
BW	−3dB Bandwidth	R_L = 50Ω	V_{CC}= 3.3V		800		MHz
MIC/AUDIO GROUND SWITCH							
t_{delay_MIC}	MIC Switch Turn On Delay Time	SBUx = 1V, R_L = 50Ω	V_{CC}= 3.3V		75		μs
t_{rise_MIC}	MIC Switch Turn On Rising Time (Note 1)				120		
t_{delay_AGND}	AGND Switch Turn On Time	SBUx pulled up to 0.5V by 16Ω, AGND connect to GND			1		ms
t_{rise_AGND}	AGND Switch Turn On Rising Time (Note 1)				1.5		
t_{OFF_MIC}	MIC Switch Turn Off Time	SBUx =2.5V, R_L =50Ω			6		μs
$t_{OFF\_Audio\ GND}$	AGND Switch Turn Off Time	SBUx: Isource=10mA, clamp to 2.5V			65		μs
BW	MIC Switch Bandwidth	R_L = 50Ω			60		MHz
SBUx_H SWITCH							
t_{ON}	SBUx_H Switch Turn On Time	SBUx= 2.5V, R_L= 50Ω	V_{CC}= 3.3V		65		μs
t_{OFF}	SBUx_H Switch Turn Off Time				150		ns
BW	Bandwidth	R_L = 50Ω			60		MHz
t_{OVP}	SBUx Pins OVP Response Time	Vsw = 3.5V to 5.5V			0.4		μs

Note: 1. Turn on timing can be controlled by I^2C register.

I²C Specification

V_{CC}=2.7V to 5.5V, V_{CC} (Typ.) =3.3V, T_A=-40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	I²C_SCL Clock Frequency			400	kHz
$t_{HD;\ STA}$	Hold Time (Repeated) START Condition	0.6			μs
t_{LOW}	Low Period of I²C_SCL Clock	1.3			μs
t_{HIGH}	High Period of I²C_SCL Clock	0.6			μs
$t_{SU;\ STA}$	Set−up Time for Repeated START Condition	0.6			μs
$t_{HD;\ DAT}$	Data Hold Time (Note 2)	0		0.9	μs
$t_{SU;\ DAT}$	Data Set−up Time (Note 3)	100			ns
t_r	Rise Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b		300	ns
t_f	Fall Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b		300	ns
$t_{SU;\ STO}$	Set−up Time for STOP Condition	0.6			μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	1.3			μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0		50	ns

Note: 2. Guaranteed by characterization. Not production tested.

3. A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ ≥ ±250ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250ns (according to the standard−mode I²C bus specification) before the I²C_SCL line is released.

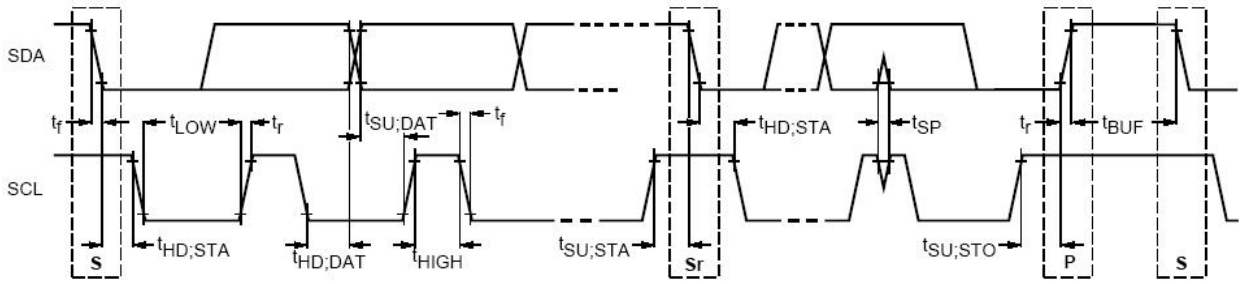


Figure 3. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

Capacitance

V_{CC}=2.7V to 5.5V, V_{CC} (Typ.) =3.3V, T_A=-40°C to 85°C, and T_A (Typ.) = 25°C.

Symbol	Parameter	Conditions	Power	Min.	Typ.	Max.	Unit
$C_{ON\_USB/Audio}$	On Capacitance (Common Port)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias	V_{CC}= 3.3V		8		pF
$C_{OFF\_USB/Audio}$	Off Capacitance (Common Port)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			6.5		pF
C_{OFF_USB}	Off Capacitance (Non−Common Ports)	f = 1MHz,100mV$_{PK-PK}$, 100mV DC bias			2.6		pF
$C_{ON\_SENSE\_SW}$	On Capacitance − (Common Ports)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			55		pF
$C_{OFF\_SENSE\_SW}$	Off Capacitance − (Common Ports)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			88		pF
$C_{ON\_MIC\_SW}$	On Capacitance − (Common Ports)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			170		pF
$C_{OFF\_MIC\_SW}$	Off Capacitance − (Common Ports)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			10		pF
$C_{ON\_AGND\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			125		pF
$C_{ON\_SBUx\_H\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV$_{PK-PK}$, 100mV DC bias			160		pF

Register Maps

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0XF5	1	1	1	1	0	1	0	1
02H	OVP Interrupt Flag	R/C	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1	OVP/ SBU2	OVP/ GSBU1	OVP/ GSBU2
03H	OVP status	R	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1	OVP/ SBU2	OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings Enable	R/W	0x98	Device Enable	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx switches
05H	Switch select	R/W	0x18	USB2 switch select	SBU1_H switches	SBU2_H switches	DN_L to DN1 or L switches	DP_R to DP1 or R switches	Sense to GSBUx	MIC to SBUx	AGND to SBUx switches
06H	Switch Status0	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	Audio Switch Left Channel turn on Control	R/W	0x01	Audio switch left channel slow control [7:0]							
09H	Audio Switch Right Channel turn on Control	R/W	0x01	Audio switch right channel slow control [7:0]							
0AH	MIC switch turn on control	R/W	0x01	MIC switch slow control [7:0]							
0BH	Sense switch turn on control	R/W	0x01	Sense switch slow control [7:0]							
0CH	Audio Ground Switch turn on Control	R/W	0x01	Audio ground switch slow control [7:0]							
0DH	Timing Delay between R switch enable and Switch On Order	R/W	0x00	Timing Delay between R switch enable and Switch On Order control [7:0]							
0EH	Timing Delay between MIC switch enable and switch on order	R/W	0x00	Timing Delay between MIC switch enable and switch on order control [7:0]							

0FH	Timing Delay between Sense switch enable and switch on order	R/W	0x00	Timing Delay between Sense switch enable and switch on order control [7:0]						
10H	Timing Delay between Audio ground switch enable and switch on order	R/W	0x00	Timing Delay between Audio ground switch enable and switch on order control [7:0]						
11H	Audio accessory status	R	0x02	Reserved					CC_IN	Reserved
12H	Function enable	R/W	0x00	OVP threshold voltage configuration	Reserved	GPIO control enable	Slow turn on control enable	MIC auto break out control enable	Reserved	Audio jack detection and configuration enable
17H	Audio jack Status	R	0x01	Reserved				4pole, SBU2 to MIC	4pole, SBU1 to MIC	3pole	No audio
18H	Moisture Detection /Audio Jack Detection/Watchdog Interrupt Flag	R	0x00	Reserved				Watchdog Timeout	Audio jack detection and configuration	Reserved
1CH	MIC detection Threshold DATA0	R/W	0x20	MIC Threshold value DATA0 [7:0]						
1DH	MIC detection Threshold DATA1	R/W	0xFF	MIC Threshold value DATA1 [7:0]						
1EH	I²C Reset	W/C	0x00	Reserved						I²C reset
1FH	Current Source Setting	R/W	0x07	Reserved				Current Source setting [3:0]		
20H	Watchdog setting	R/W	0x01	Watchdog enable	Reserved			Watchdog reset	Watchdog timer	
21H	Timing Delay between L switch enable and Switch On Order	R/W	0x00	Timing Delay between L switch enable and Switch On Order control [7:0]						

I²C Slave Address

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	0	0	0	0	1	0	R/W

Register Definition

Device ID

Address: 00h

Reset Value: 8'b 1111_0101

Type: Read

Bits	Name	Size	Description
7:6	Vendor ID	2	Vendor ID
5:3	Version ID	3	Device Version ID
2:0	Revision ID	3	Revision History ID

OVP INTERRUPT Flag

Address: 02h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
2	SBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

OVP Status

Address: 03h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	OVP on DP_R PIN	1	0: OVP event has not occurred

			1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

Switching Setting Enable

Address: 04h

Reset Value: 8'b 1001_1000

Type: Read/Write

Bits	Name	Size	Description
7	Device Enable	1	1: Device Enable. 0: Device Disable; L, R pull down by 10kΩ and other switch nodes will be high−Z for positive input. Device Enable = 1 Device enable = 0 ENN = 1 Device Disable Device Disable ENN = 0 Device Enable Device Disable
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high−Z for positive input 1: Switch Enable
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high−Z for positive input 1: Switch Enable
4	DN_L to DN1/2 or L switches	1	0: Switch Disable; DN_L, DN1/2 will be high−Z for positive input. L pull down by 10kΩ 1: Switch Enable
3	DP_R to DP1/2 or R switches	1	0: Switch Disable; DP_R, DP1/2 will be high−Z for positive input. R pull down by 10kΩ 1: Switch Enable
2	Sense to GSBUx switches	1	0: Switch Disable; Sense,GSBU1 and GSBU2 will be high−Z for positive input 1: Switch Enable
1	MIC to SBUx switches	1	0: Switch Disable: MIC will be high−Z for positive input. 1: Switch Enable
0	AGND to SBUx switches	1	0: Switch Disable: AGND will be high−Z for positive input. 1: Switch Enable

Switch Select

Address: 05h

Reset Value: 8'b 0001_1000

Type: Read/Write

Bits	Name	Size	Description
7	USB2 switch select	1	0: USB2 off. USB1,Audio switch depend on 05h,bit<4:3> and 04h,bit<4:3> 1: DP/R~DP2, DN/L~DN2 switches ON, when 04h, bit<4:3> ='11'
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN1 or L switches	1	0: DN_L to L switch ON 1: DN_L to DN1 switch ON
3	DP_R to DP1 or R switches	1	0: DP_R to R switch ON 1: DP_R to DP1 switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

Switch Status0

Address: 06h

Reset Value: 8'b 0000_0101

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:2]	Sense Switch Status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not Valid
[3:2]	DP_R Switch Status	2	00: DP_R Switch Open/Not Connected 01: DP_R connected to DP1 10: DP_R connected to R 11: DP_R connected to DP2
[1:0]	DN_L switch Status	2	00: DN_L Switch Open/Not Connected 01: DN_L connected to DN1 10: DN_L connected to L 11: DN_L connected to DN2

Switch Status1

Address: 07h

Reset Value: 8'b 0000_0000

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 Switch Status	3	000: SBU2 switch is Open/Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 Switch Status	3	000: SBU1 switch is Open/Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

Audio Switch Left Channel Slow Turn-on

Address: 08h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111:25600μs
			…
			00000001: 200μs
			00000000: 100μs

Audio Switch Right Channel Slow Turn-on

Address: 09h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600μs
			…
			00000001: 200μs
			00000000: 100μs

MIC Switch Slow Turn-on

Address: 0Ah

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25700μs
			…
			00000010: 350μs
			00000001: 250μs
			00000000: Not Valid

Sense Switch Slow Turn-on

Address: 0Bh

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600μs
			…
			00000001: 200μs
			00000000: 100μs

Audio Ground Switch Slow Turn-on

Address: 0Ch

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 179000μs
			…
			00000001: 1400μs
			00000000: 700μs

Timing Delay Between R Switch Enable And Switch On Order

Address: 0Dh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102ms
			11111110: 101.6ms
			…
			00000001: 400μs
			00000000: 0μs

Timing Delay Between MIC Switch Enable And Switch On Order

Address: 0Eh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102ms
			11111110: 101.6μs
			…
			00000001: 400μs
			00000000: 0μs

Timing Delay Between Sense Switch Enable And Switch On Order

Address: 0Fh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102ms
			11111110:101.6ms
			…
			00000001: 400μs
			00000000: 0μs

Timing Delay Between Audio Ground Switch Enable And Switch On Order

Address: 10h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102ms
			11111110: 101.6ms
			…
			00000001: 400μs
			00000000: 0μs

Audio Accessory Status

Address: 11h

Reset Value: 8'b 0000_0010

Type: Read/Write

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2V 1: CC_IN > 1.5V
0	Reserved	1	Do not use

Function Enable

Address: 12h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:6]	OVP threshold voltage configuration	2	00: 4.4V 01: 4.6V 10: 4.8V 11: 5.0V
5	Reserved	1	Do not use
4	GPIO control enable	1	Do not use
3	Slow turn on control enable	1	1: enable 0: disable
2	MIC auto break out control enable	1	1: enable 0: disable
1	Reserved	1	Do not use
0	Audio jack detection and configuration enable	1	1: enable; will be changed to '0' after audio jack detection and configuration 0: disable

When GPIO control mode (manual switch control) is enable. '**Switch control'** register is changed to read only.

Audio Jack Status

Address: 17h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	4pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4pole	1	1: 4 Pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3pole	1	1: 3 pole 0: others
0	No audio accessory	1	1: No audio accessory 0: Audio accessory attached

Moisture Detection/Audio Jack Detection/Watchdog Interrupt Flag

Address: 18h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
3	Watchdog Timeout	1	0: Watchdog timeout has not occurred 1: Watchdog timeout has occurred

2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
[1:0]	Reserved	2	Do Not Use

MIC Detection Threshold Data0

Address: 1Ch

Reset Value: 8'b 0010_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300mV

MIC Detection Threshold Data1

Address: 1Dh

Reset Value: 8'b 1111_1111

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4V

I²C Reset

Address: 1Eh

Reset Value: 8'b 0000_0000

Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I²C reset	1	0: default 1: I²C reset

Current Source Setting

Address: 1Fh

Reset Value: 8'b 0000_0111

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current Source Setting	4	1111: 1500μA 0111: 700μA 0001: 100μA 0000: invalid

Watchdog setting

Address: 20h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
7	Watchdog enable	1	0: Watchdog disabled 1: Watchdog enabled
[6:4]	Reserved	3	Reserved
3	Watchdog reset	1	
[2:0]	Watchdog timer	3	000: 0.5s 001: 1s 010: 2s 011: 5s 100: 10s 101: 30s 110: 60s 111: 5min

Note: When WD is enabled, if watchdog reset(20h,bit<3>)=0,IC will reset to USB1 state per 1s(configured by bit<2:0>).

Timing Delay Between L Switch Enable And Switch On Order

Address: 21h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102ms
			11111110: 101.6ms
			…
			00000001: 400μs
			00000000: 0μs

Application Information

Over-Voltage Protection

DIO4483 features over−voltage protection (OVP) on receptacle side pins that turns off the internal signal routing path if the voltage exceeds the OVP threshold. If OVP is occurred, flag register 0x02h and 0x03h will indicate which pin had OVP event. OVP threshold voltage is configurable by 0x12h, bit [7:6].

Headset Detection

DIO4483 integrates headset unplug detection function by detecting the CC_IN voltage. The function will be active when device is enabling. Register 0x11h, bit[1:0] Output can indicate if CC_IN is low (CC_IN<1.2V) or high(CC_IN>1.5V).

	0x11h, bit [1]	0x11h, bit [0]
CC_IN <1.2V	0	1
CC_IN > 1.5V	1	0

MIC Switch Auto−off Function

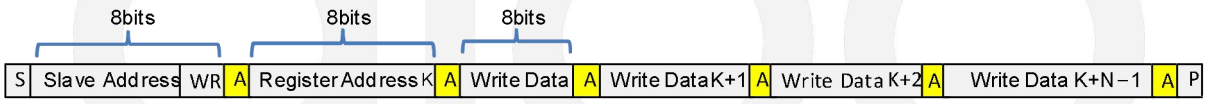
The function is active during control bit 0x12h bit [2] = 1. When CC_IN is changed from low to high, and L, R, AGND switches are under on status, MIC switch will be off and receptacle side pin will be pulled to ground for 50μs first. Then it shows high−Z status under MIC switch is set on status.

Audio Jack Detection and Configuration

The function is active when control bit 0x12h bit [0] = 1. When the headset is inserted, DIO4483 can detect OMTP, CTIA or 3-Pole headset and configurate pinout automatically. During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R, L, MIC, Sense and AGND switches will turn on according to detection results and timing control setting.

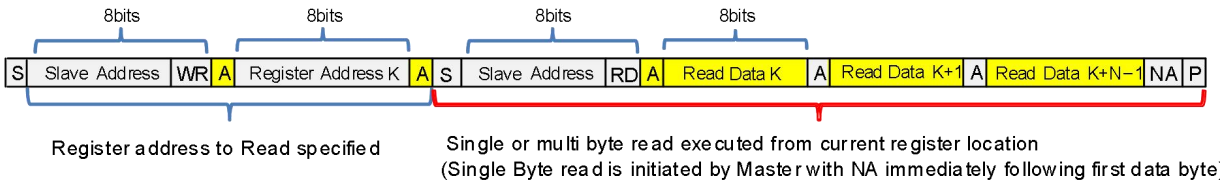
I²C Interface

The DIO4483 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400kHz, signals. Examples of an I²C write and read sequence are shown in below figures respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 4. I²C Write Example



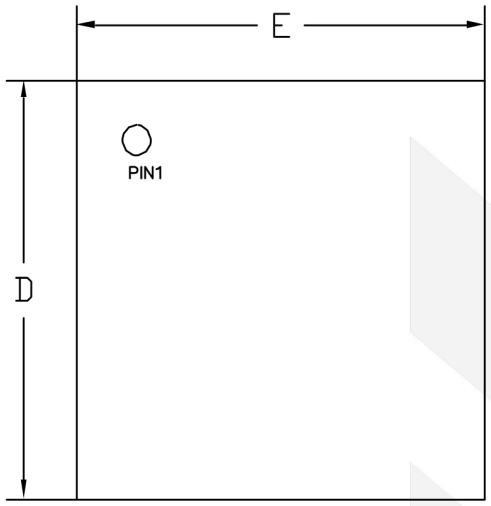
NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

From Master to Slave
From Slave to Master

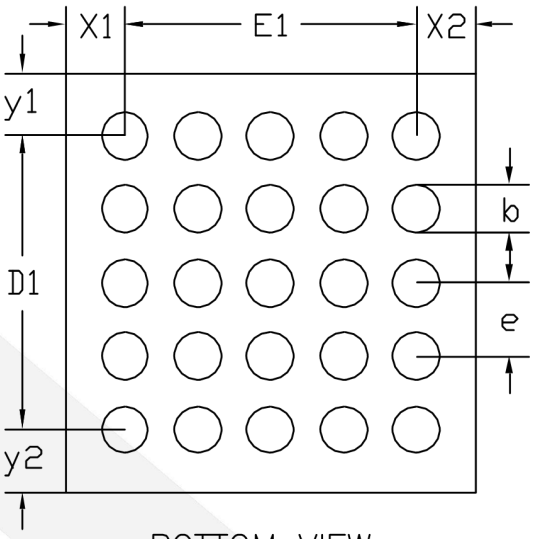
S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write = 0
RD Read = 1
P Stop Condition

Figure 5. I²C Read Example

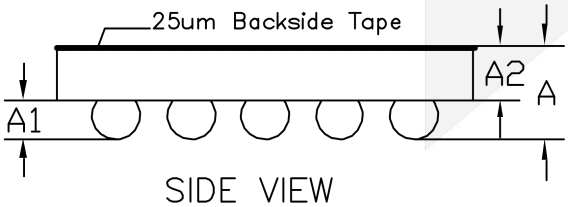
Physical Dimensions: WLCSP-25



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	**MIN**	**NOM**	**MAX**
A	0.547	0.586	0.625
A1	0.190	0.210	0.230
A2	0.351	0.376	0.401
D	2.250	2.280	2.310
D1		1.600 BSC	
E	2.210	2.240	2.270
E1		1.600 BSC	
b	0.238	0.258	0.278
e		0.400 BSC	
x1		0.320 REF	
x2		0.320 REF	
y1		0.340 REF	
y2		0.340 REF	

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as, cell phone, handheld products, laptop, and medical equipment and so on. Dioo's product families include analog signal processing and amplifying, LED drivers and charger IC. Go to http://www.dioo.com for a complete list of Dioo product families.

For additional product information, or full datasheet, please contact with our Sales Department or Representatives.