ACM3221 3W Mono, Analog Input High Performance & Ultra Low Power Class-D Audio Amplifier

1. Features

- **Single Supply Voltage**
  - PVDD: 2.5V to 5.5V
- **Various Output Configurations**
  - 1×2.4W, 1% THD+N, 5V, 4Ω
  - 1×1.4W, 1% THD+N, 5V, 8Ω
- **Excellent Audio Performance**
  - THD+N ≤ 0.05% at 10mW, 1kHz, PVDD = 3.7V
  - Idle switching A-weighted noise ≤ 12 uV_{RMS}
  - <=1mV output DC offset
  - 93% efficient @1.7W Pout, 8Ω
  - Low Idle Current: <1.2mA, PVDD=3.7V
  - Click-and-Pop Suppression
- **Low EMI Technology**
  - Spread Spectrum Supported
- **Gain Management**
  - 12dB, 9dB, 6dB, 3dB and 0dB fixed gain setting
- **Protections**
  - Thermal and Overcurrent Protection
  - Under-Voltage detection

2. Applications

- Cellular Phones/Watches
- Tablets
- Portable Audio Players
- TWS/OWS Headsets
- VR/AR Glasses

3. General Description

The ACM3221 mono 3W Class D amplifier provides excellent audio performance with high efficiency and low power. This device offers five selectable gain settings (0dB, 3dB, 6dB, 9dB and 12dB) set by a single gain-select input (GAIN).

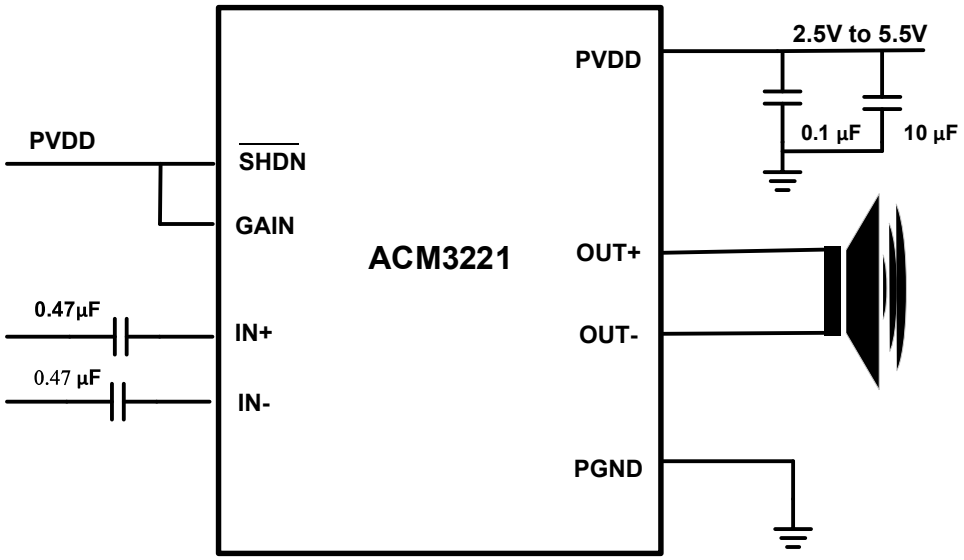
Active emissions-limiting, edge-rate, and overshoot control circuitry greatly reduces EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices. These features reduce application component count. The device consumes <1.2mA at 3.7V (1.5mA at 5V) quiescent current extends battery life in portable applications.

The IC is available in a 9-bump (0.9mm x 0.9mm) WLP with 0.3mm pitch and 8 Pin (2.0mm x 2.0mm) DFN which are specified over the extended -40℃ to +85℃ temperature range.

4. Device Information

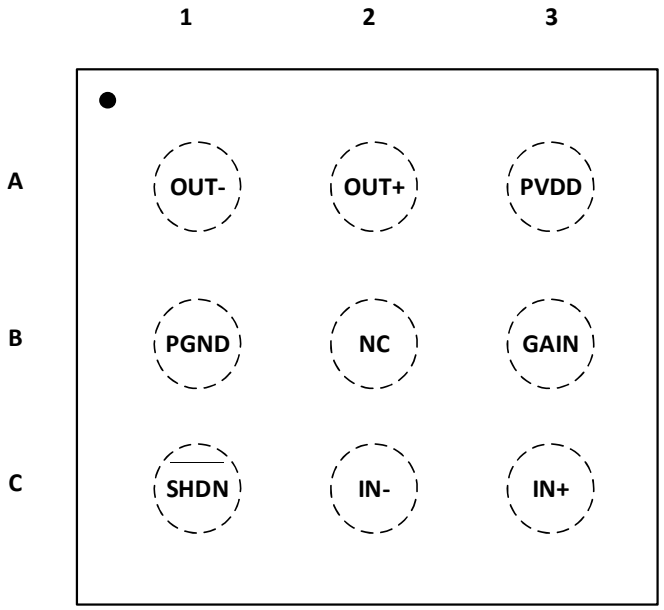
Part number	Package	Body size
ACM3221	WLP9D	0.9 mm × 0.9 mm
ACM3221	DFN8L	2.0 mm × 2.0 mm

- **Simplified Application Circuit**



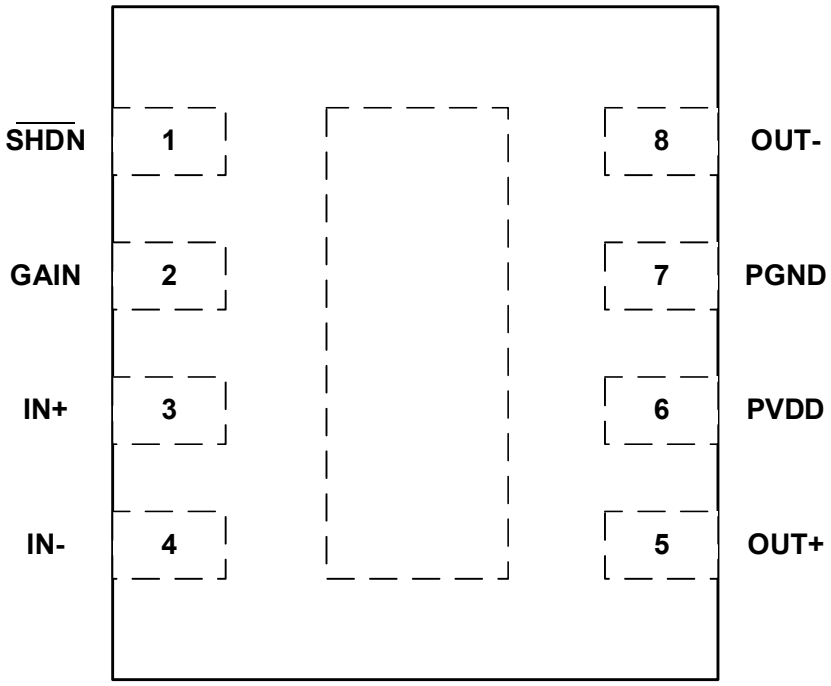
5. Pin Configuration and Function Descriptions

ACM3221
WLP9



Pin No.	Name	Type	Description
A1	OUT-	AO	Negative audio output
A2	OUT+	AO	Positive audio output
A3	PVDD	PWR	Power Supply:2.5V to 5.5V
B1	PGND	PWR	Power Ground
B2	NC		NC
B3	GAIN	AIN	GAIN Selection
C1	$\overline{\text{SHDN}}$	DIN	Active-Low Shutdown Input
C2	IN-	AIN	Negative audio input
C3	IN+	AIN	Positive audio input

ACM3221
DFN8L



Pin No.	Name	Type	Description
1	$\overline{SHDN}$	AIN	Active-Low Shutdown Input
2	GAIN	AIN	GAIN Selection
3	IN+	AIN	Positive audio input
4	IN-	AIN	Negative audio input
5	OUT+	AO	Positive audio output
6	PVDD	PWR	Power Supply:2.5V to 5.5V
7	PGND	PWR	Power Ground
8	OUT-	AO	Negative audio output

6. Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
PVDD	Supply Voltage	-0.3	6	V
Input Voltage, VI	IN+, IN-	-0.3	PVDD+0.3	V
	GAIN	-0.3	PVDD+0.3	V
	$\overline{SHDN}$	-0.3	PVDD+0.3	V
TA	Ambient operating temperature	-40	85	℃
TJ	Operating junction temperature	-40	160	℃
Tstg	Storage temperature	-40	125	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicted under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001-2017 (1)	+2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2018 (2)	+500	

(1) JEDEC document JS-001-2017 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JS-002-2018 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
V(SUPLLY)	Power supply inputs	PVDD	2.5		5.5	V
VIH	High-level input voltage	GAIN	1.4			V
VIL	Low-level input voltage	GAIN			0.4	
VOL	Low-level output voltage	$\overline{SHDN}$			0.8	V
IIH	High-level input current				50	μA
IIL	Low-level input current				5	μA
RL	Minimum load Impedance		3.2	4		Ω
TJ	Junction Operating Temperature		-40		160	℃
TA	Ambient Operating Temperature		-40		85	℃

6.4 Thermal Information

		ACM3221, WLP 9 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
θJA	Junction-to-ambient thermal resistance	TBD	℃/W
θJT	Junction-to-case (top) thermal resistance	TBD	℃/W
ψJT	Junction-to-top characterization parameter	TBD	℃/W

		ACM3221, DFN 8 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
θJA	Junction-to-ambient thermal resistance	70	℃/W
θJT	Junction-to-case (top) thermal resistance	TBD	℃/W
ψJT	Junction-to-top characterization parameter	TBD	℃/W

6.5 Electrical Characteristics

PVDD=5V, Fin=1kHz, Load=8Ω+33uH, free-are room temperature 25℃, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVDD	Supply Voltage Range	Inferred from PSRR test	2.5		5.5	V
UVLO	Undervoltage Lockout	PVDD falling		2.2		V
		PVDD = 3.7V		1.15		mA

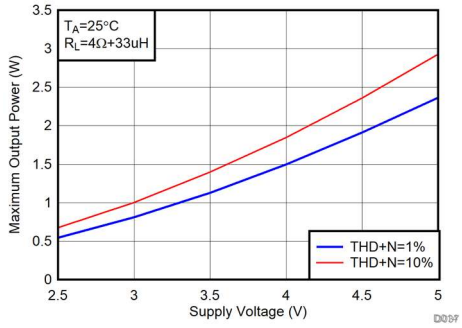
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISHDN	Shutdown Supply Current	$\overline{SHDN}$ = 0V, TA = +25℃			<0.1	10	uA
tON	Turn-On Time				6		mS
VBIAS	Bias Voltage				PVDD/2		V
RIN	Input Resistance	Av=12dB			25		kΩ
		Av=9dB			35		
		Av=6dB			50		
		Av=3dB			71		
		Av=0dB			99		
Av	Voltage Gain	Connect GAIN to PGND		11.5	12	12.5	dB
		Connect GAIN to PGND through 100 kΩ		8.5	9	9.5	
		Connect GAIN to PVDD		5.5	6	6.5	
		Connect GAIN to PVDD through 100 kΩ		2.5	3	3.5	
		Floating		-0.5	0	0.5	
VOS	Output Offset Voltage	TA = +25℃			1		mV
KCP	Click and Pop	Peak voltage, A-weighted, 32 samples per second, RL = 8Ω			-74		dBV
					-60		
CMRR	Common-Mode Rejection Ratio	fIN = 1kHz, input referred			80		dB
PSRR	Power-Supply Rejection Ratio	PVDD=2.5V to 5.5V, TA = +25℃		72	90		dB
		VRIPPLE= 200mVP-P	f = 217Hz		80		
			f = 1kHz		84		
			f = 20kHz		84		
POUT	Output Power (Speaker Mode)	THD+N = 10%, f = 1kHz, RL = 4Ω + 33uH	PVDD = 5.0V		3.0		W
			PVDD = 4.2V		2.1		
			PVDD = 3.7V		1.6		
		THD+N = 1%, f = 1kHz, RL = 4Ω + 33uH	PVDD = 5.0V		2.4		
			PVDD = 4.2V		1.7		
			PVDD = 3.7V		1.3		
		THD+N = 10%, f = 1kHz, RL = 8Ω + 33uH	PVDD = 5.0V		1.7		
			PVDD = 4.2V		1.2		
			PVDD = 3.7V		0.93		
		THD+N = 1%, f = 1kHz, RL = 8Ω + 33uH	PVDD = 5.0V		1.4		
			PVDD = 4.2V		0.97		
			PVDD = 3.7V		0.75		
POUT	Output Power (Headphone Mode)	THD+N = 1%, f = 1kHz, RL = 16Ω	PVDD = 4.2V		527		mW
			PVDD = 3.7V		410		
		THD+N = 1%, f = 1kHz, RL = 32Ω	PVDD = 4.2V		275		
			PVDD = 3.7V		213		
THD+N	Total Harmonic Distortion Plus Noise	fIN = 1kHz	RL = 4Ω POUT = 0.1W		0.1		%
			RL = 8Ω POUT = 0.1W		0.1		
			RL = 16Ω POUT =0.01W		0.05		
			RL = 32Ω POUT = 0.01W		0.05		
fOSC	Oscillator Frequency				320		kHz

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
η	Efficiency	POUT = 1.7W, RL = 8Ω			93		%
	Spread-Spectrum Bandwidth				12		kHz
VN	Noise	A-weighted	Av=12dB		20		uV
			Av=9dB		17		
			Av=6dB		15		
			Av=3dB		13		
			Av=0dB		12		
ILIM	Output Current Limit				2.5		A
	Thermal Shutdown Level				160		℃
	Thermal Shutdown Hysteresis				15		℃
DIGITAL INPUT							
VINH	Input-Voltage High	PVDD = 2.5V to 5.5V		1.4			V
VINL	Input-Voltage Low	PVDD = 2.5V to 5.5V				0.4	
	Input Leakage Current	TA = +25℃				1	uA

7. Typical Characteristics

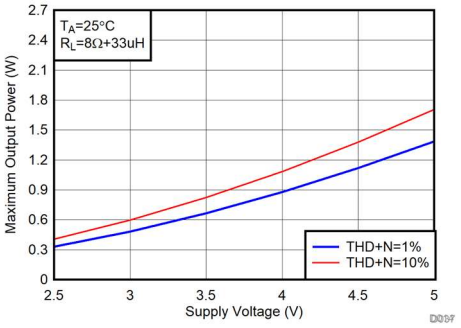
7.1 Typical Audio Performance Curves

Free-air room temperature 25℃ (unless otherwise noted.) Measurements were made using ACM3221 EVM board and Audio Precision System APX5xx Series with Analog Analyzer filter set to 20kHz Low Pass filter.



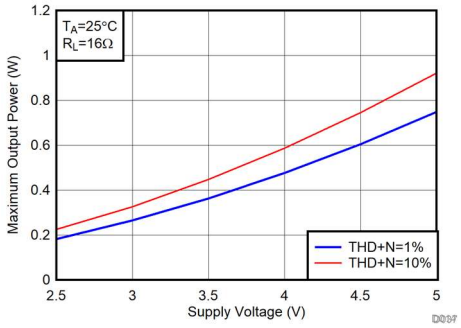
(Load=4Ω+33uH, Fsw=320kHz)

Figure 1 Output Power vs PVDD



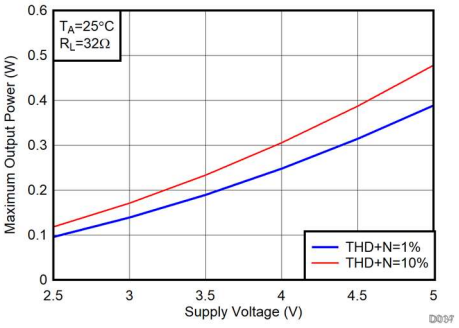
(Load=8Ω+33uH, Fsw=320kHz)

Figure 2 Output Power vs PVDD



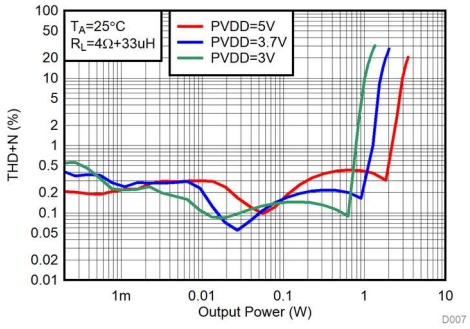
(Load=16Ω, Fsw=320kHz)

Figure 3 Output Power vs PVDD



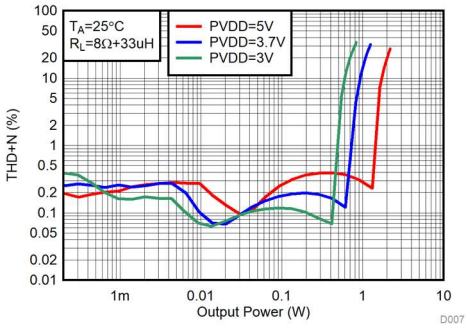
(Load=32Ω, Fsw=320kHz)

Figure 4 Output Power vs PVDD



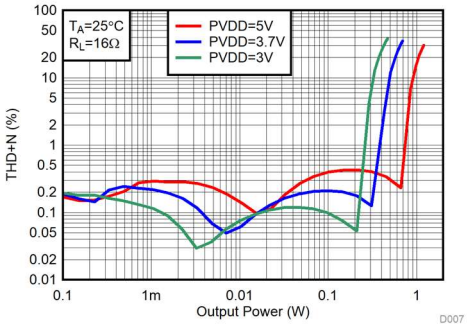
(Load=4Ω+33uH, Fsw=320kHz)

Figure 5 THD+N vs Output Power



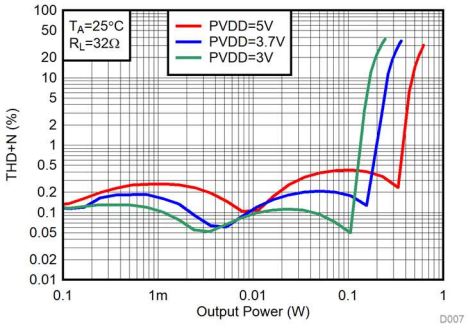
(Load=8Ω+33uH, Fsw=320kHz)

Figure 6 THD+N vs Output Power



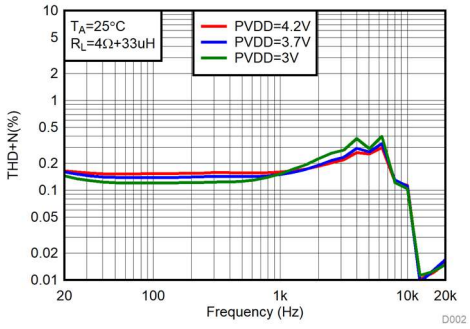
(Load=16Ω, Fsw=320kHz)

Figure 7 THD+N vs Output Power



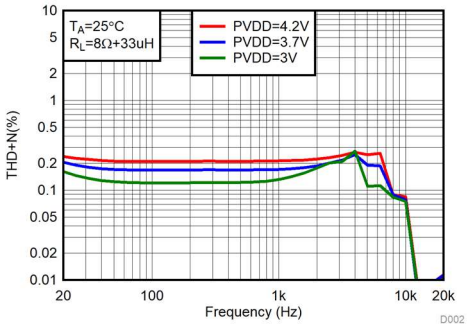
(Load=32Ω, Fsw=320kHz)

Figure 8 THD+N vs Output Power



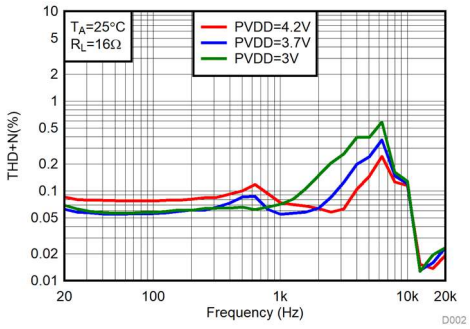
(Load=4Ω+33uH, Pout=0.1W, Fsw=320kHz)

Figure 9 THD+N vs Frequency



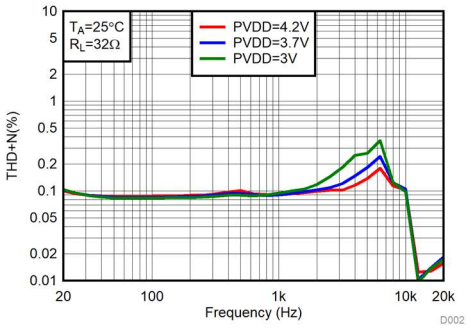
(Load=8Ω+33uH, Pout=0.1W, Fsw=320kHz)

Figure 10 THD+N vs Frequency



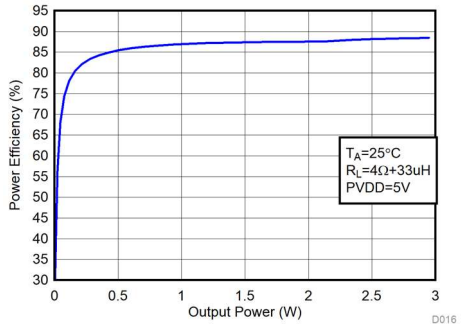
(Load=16Ω, Pout=10mW, Fsw=320kHz)

Figure 11 THD+N vs Frequency



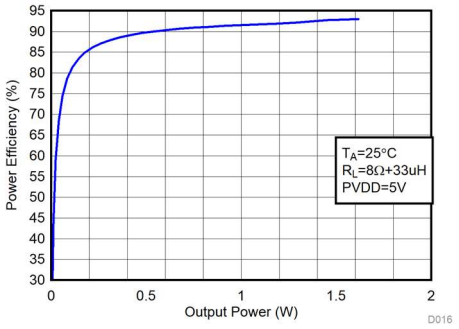
(Load=32Ω, Pout=10mW, Fsw=320kHz)

Figure 12 THD+N vs Frequency



(Load=4Ω+33uH, Fsw=320kHz, PVDD=5V)

Figure 13 Efficiency



(Load=8Ω+33uH, Fsw=320kHz, PVDD=5V)

Figure 14 Efficiency

8. Detailed Description

8.1 Overview

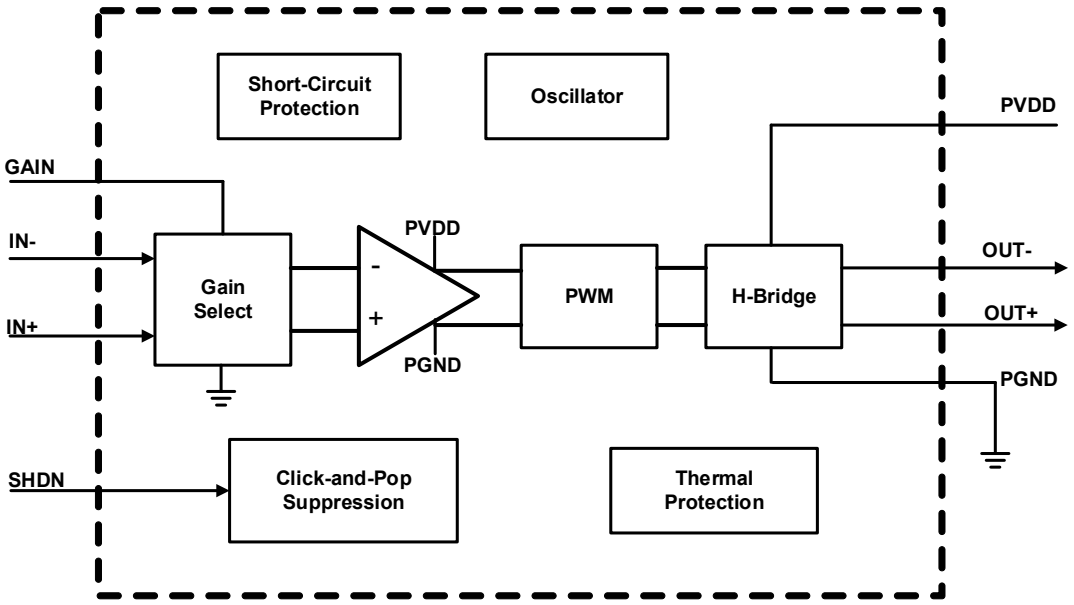
The ACM3221 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The device offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal overload and short-circuit protection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Gain Setting

The ACM3221 offers five programmable gain selections through a single gain input (GAIN).

Table 1 Gain Setting

GAIN Configuration	AMPLIFIER GAIN
Connect to PGND	12 dB
Connect to PGND through 100kΩ resistor	9 dB
Connect to PVDD	6 dB
Connect to PVDD through 100kΩ resistor	3dB
Unconnected	0dB

8.3.2 Component Selection

Decoupling Capacitors

The ACM3221 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor 0.1 μF, placed as close as possible to the device PVDD lead works best. Placing this capacitor close to the ACM3221 is important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the devices and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 μF or greater capacitor is placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device. Typically, the smaller the capacitor's case size, the lower the inductance and the closer it can be placed to the ACM3221. X5R and X7R dielectric capacitors are recommended for both of these two capacitors.

Input Capacitors

The input-coupling capacitor, in conjunction with the amplifier's internal input resistance (RIN), forms a high-pass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level. capacitor CI and the input resistance RI (typically 100 kΩ) of the ACM3221 is given by Equation below:

$$f_C = \frac{1}{2\pi R_L C_O}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speaker response may also be taken into consideration when setting the corner frequency using input capacitors. Solving for the input coupling capacitance, we get:

$$C_O = \frac{1}{2\pi R_L f_C}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

8.3.3 Shutdown (SHDN) control

Pulling SHDN pin low will let ACM3221 operate in low-current state for power conservation. The ACM3221 outputs will enter mute once SHDN pin is pulled low, and regulator will also disable to save power. If let SHDN pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance,

place the chip in the shutdown mode in advance of removing the power supply.

8.3.4 Eliminating Turn-on Pop and Power Supply Sequencing

The ACM3221 has excellent noise and turn-on/turn-off pop performance. It uses and integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5ms.

ACM3221 keeps the output DC voltage at 0V even when the amplifier is powered up. The active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the ACM3221 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the ACM3221 before deactivating the audio input source. The SHDN pin controls device shutdown, set to 0.6V or lower to deactivate the ACM3221, set to 1.3V or higher to activate.

8.3.5 Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2.5A typical), the IC disables the outputs for approximately 80mS. At the end of 80mS, the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenable the outputs until the fault condition is removed.

8.3.6 Thermal Protection

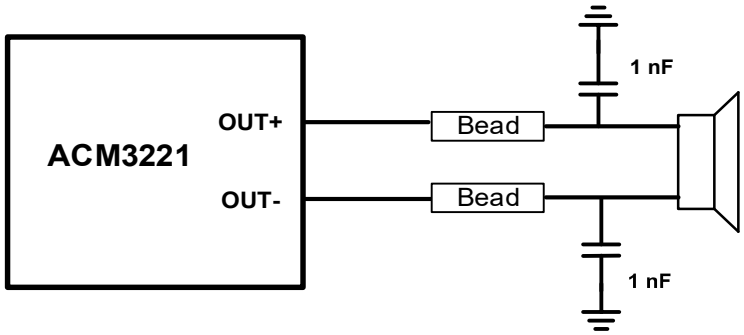
The ACM3221 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Note that the use of speakers less resistive than 4 Ω (typical) is not advisable. Below 4 Ω (typical) the thermal performance of the device dramatically reduces because of increased output current and reduced amplifier efficiency. The Absolute Maximum rating of 3.2 Ω covers the manufacturing tolerance of a 4 Ω speaker and speaker impedance decrease due to frequency.

8.3.7 Under Voltage Protection

Once the PVDD voltage drop below the 2.2V Typical, device will set the output driver from Play mode to Hi-Z mode. Once PVDD rise above 2.5V (Typical), device will come back to Play mode.

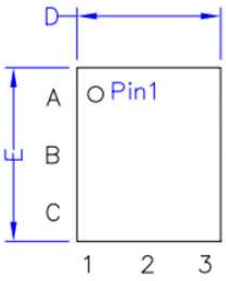
8.3.8 Filterless Class-D

Traditional Class D amplifiers require an output filter. The filter adds cost, size, and decreases efficiency and THD+N performance. The IC's filterless modulation scheme does not require an output filter. In case of long distance output terminal pin to speaker or there is EMI sensitive device nearby, bead and capacitor filter is recommended adding close to ACM3221 output terminal pins.

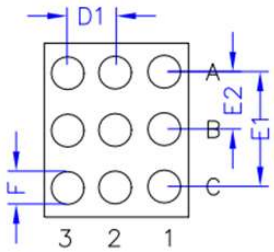


9 Package Dimensions

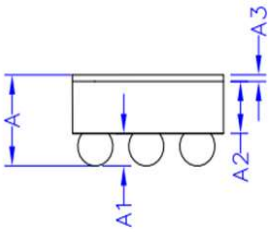
Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM3221	WLP Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM3221



TOP VIEW
Ball Down



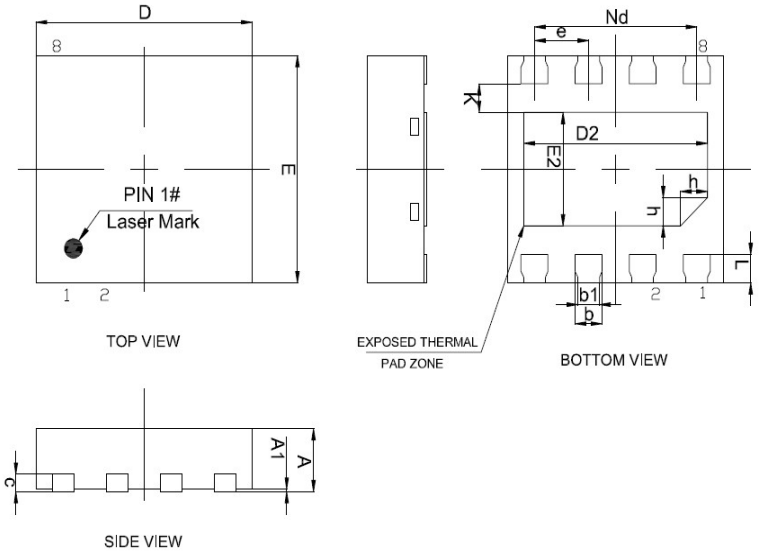
BOTTOM VIEW
Ball Up



SIDE VIEW

				Unit:mm
		NO.	Mean	Tolarence
Total Thickness		A	0.599	±0.0375
Ball Height+UBM Thickness		A1	0.119	±0.020
Wafer/Grinding Thickness		A2	0.455	±0.0125
Backside Coating Thickness		A3	0.025	±0.005
Pkg Die Size	X	D	0.895	±0.025
	Y	E	0.895	±0.025
Ball Size afer reflow		F	0.168	±0.020
Ball Pitch		D1	0.3	NA
		E1	0.6	NA
		E2	0.3	NA

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM3221	DFN Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM3221



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.20REF		
c	0.152REF		
D	1.90	2.00	2.10
D2	1.60	1.70	1.80
e	0.50BSC		
Nd	1.50BSC		
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
L	0.20	0.25	0.30
h	0.20	0.25	0.30
K	0.25REF		