# Zbit 128GB eMMC5.1 Datasheet

# ZBEM128G03RIF1

**Rev 1.0**

# Overview

■ **eMMC 5.1 specification compatibility**

- Compatible to eMMC 4.41/4.51/5.0

■ **Bus mode**
- Data bus width: 1 bit (default), 4 bits, 8 bits
- Data transfer rate: up to 310MB/s (HS400)
- Timing mode: SDR/DDR/HS200/HS400
- I/F boot frequency: 0 ~ 52 MHz
- I/F clock frequency: 0 ~ 200 MHz

■ **Operating voltage range**
- VCC: 2.7 ~ 3.6V
- VCCQ: 1.7 ~ 1.95V or 2.7 ~ 3.6V

■ **Temperature**
- Operating temperature: -25 ~ 85℃
- Storage temperature: -45 ~ 85℃

■ **Support feature**
- RPMB - Boot partition
- Write protection
- Erase, discard, trim, sanitize
- HPI
- Background operations
- Device health report
- Field firmware update (FFU)
- Sleep / awake
- Packed command
- Support Hardware ECC engine
- Support auto power save mode
- Preventing from sudden-power-off

Zbit reserves the right to change specifications without notice.

# Revision History

| Rev | Date | History |
|-----|------|---------|
| V1.0 | 2024/2/28 | Initial |
| | | |
| | | |
| | | |

# Contents

# 1. Intrduction

## 1.1 General Description

Zbit eMMC device consists of NAND flash and a built-in MMC controller. This product is a high performance and quality embedded storage solution and compatible with JEDEC standard eMMC5.1 specification. Its strong ECC engine significantly improves error correction enabling longer device lifetime and an increased ability to handle higher raw bit error rate. The eMMC controller and software directly manage NAND flash, including ECC, wear-leveling, bad block management, garbage collection and performance optimization, and manage interface protocols. This architecture insulates any revision of NAND flash from the eMMC Host, makes the device easy to integrate and accelerates time-to-market.

## 1.2 Part Number



**ZB  EM  128G  03  R  I  F1**

*ZB*：Zbit

*Product Family*：
EM：EMMC

*Density*：
08G: 8GB
16G: 16GB
32G: 32GB
64G: 64GB
128G: 128GB

*Generation*：
01: 1st version
02: 2nd version
03: 3rd version
…

*Controller Generating*：
F1: A controller

*Temperature Range*：
I: -20°C-85°C;
J: -40°C-85°C;

*Package Type*：
R: BGA153 11.5*13*1.0mm
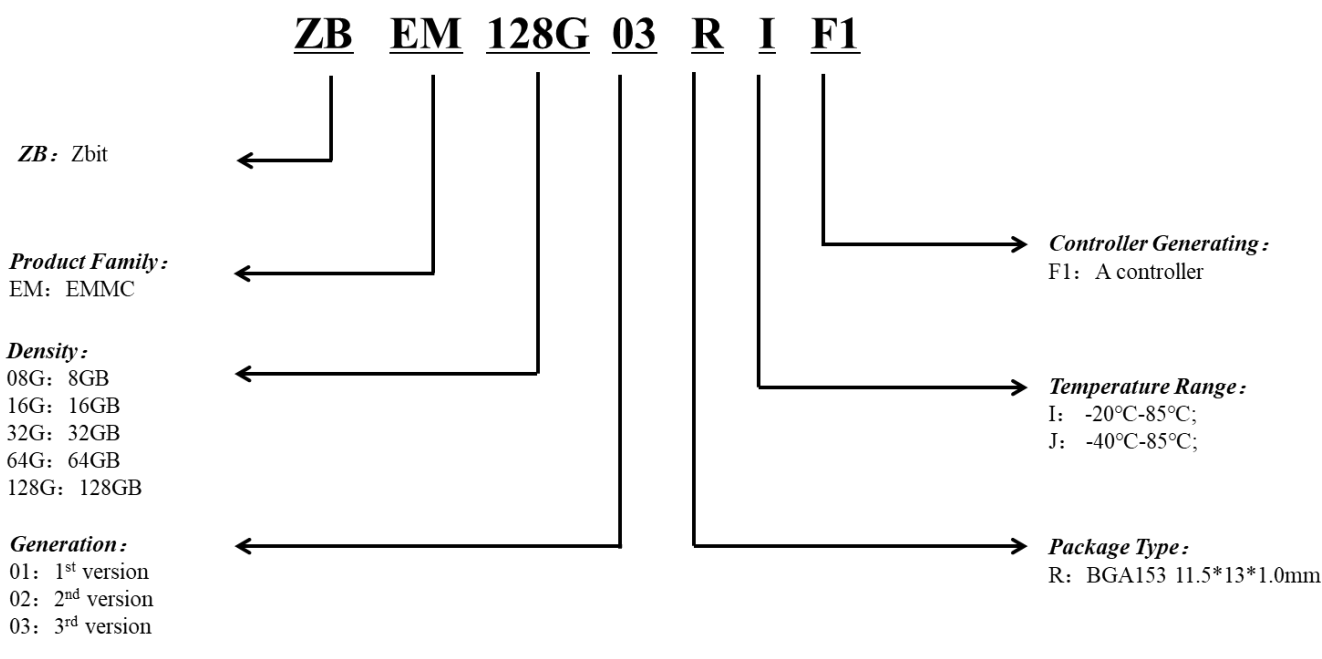
## 1.3 Ordering Information

Please contact Zbit regional sales for the latest product selection and available form factors.

Table 1 Ordering Information

| Part Number | Density | Package Type | Package Dimensions | Shipping |
|---|---|---|---|---|
| ZBEM128G03RIF1 | 128GB | BGA153 | 11.5*13*1.0mm$^3$ | Tray |

# 2. Package Configuration

## 2.1 Pin Assignments
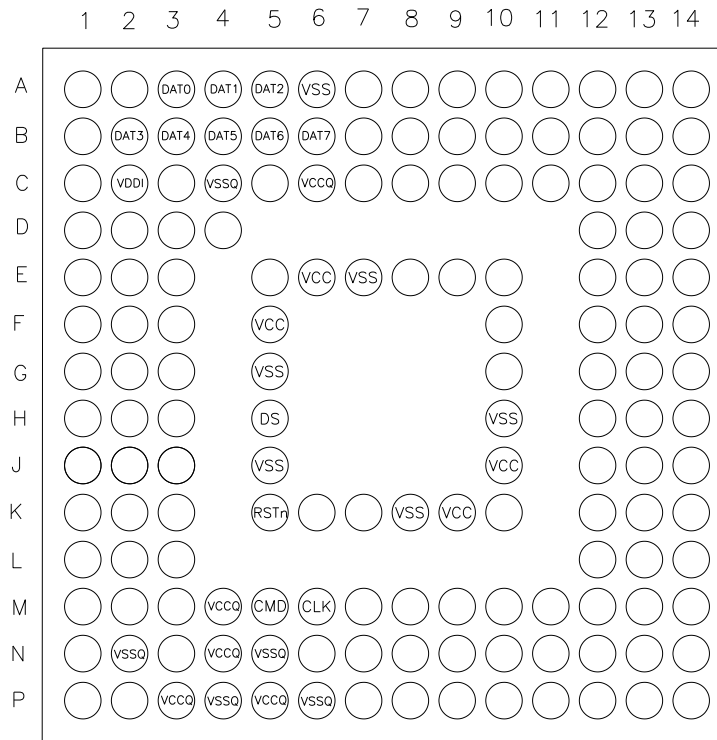


Figure 1. Ball Mapping

## 2.2 Signal Definition

Table 2. Ball & Signal Assignment

| Signal | Type | Description |
|--------|------|-------------|
| DAT0 | I/O | Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT [3:0] (4-bit mode) or DAT [7:0] (8-bit mode). eMMC includes internal pull-up resistors for data lines DAT [7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT [3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT [7:1] lines. |
| DAT1 | I/O | |
| DAT2 | I/O | |
| DAT3 | I/O | |
| DAT4 | I/O | |

| Signal | Type | Description |
|--------|------|-------------|
| DAT5 | I/O | |
| DAT6 | I/O | |
| DAT7 | I/O | |
| CMD | I/O | Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host. |
| CLK | I | Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency. |
| RST_n | I | Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set EXT_CSD register byte 162, bits [1:0] to 0x1 to enable this functionality before the host can use it. |
| DS | O | Data strobe: Generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycle of this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the other bit for the negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and is "Don't Care" on the negative edge. |
| VCC | P | VCC: NAND interface I/O and NAND Flash power supply |
| VCCQ | P | VCCQ: eMMC controller core and eMMC I/F I/O power supply. |
| VSS | P | VSS: NAND interface I/O and NAND Flash ground connection. |
| VSSQ | P | VSSQ: eMMC controller core and eMMC I/F ground connection. |
| VDDI | - | Internal voltage node. |

**Note:**

1) I/O = Bi-direction, I = Input, O = Output, P = Power/Analog
2) VSS and VSSQ are connected internally.

## 2.3 Package Dimension
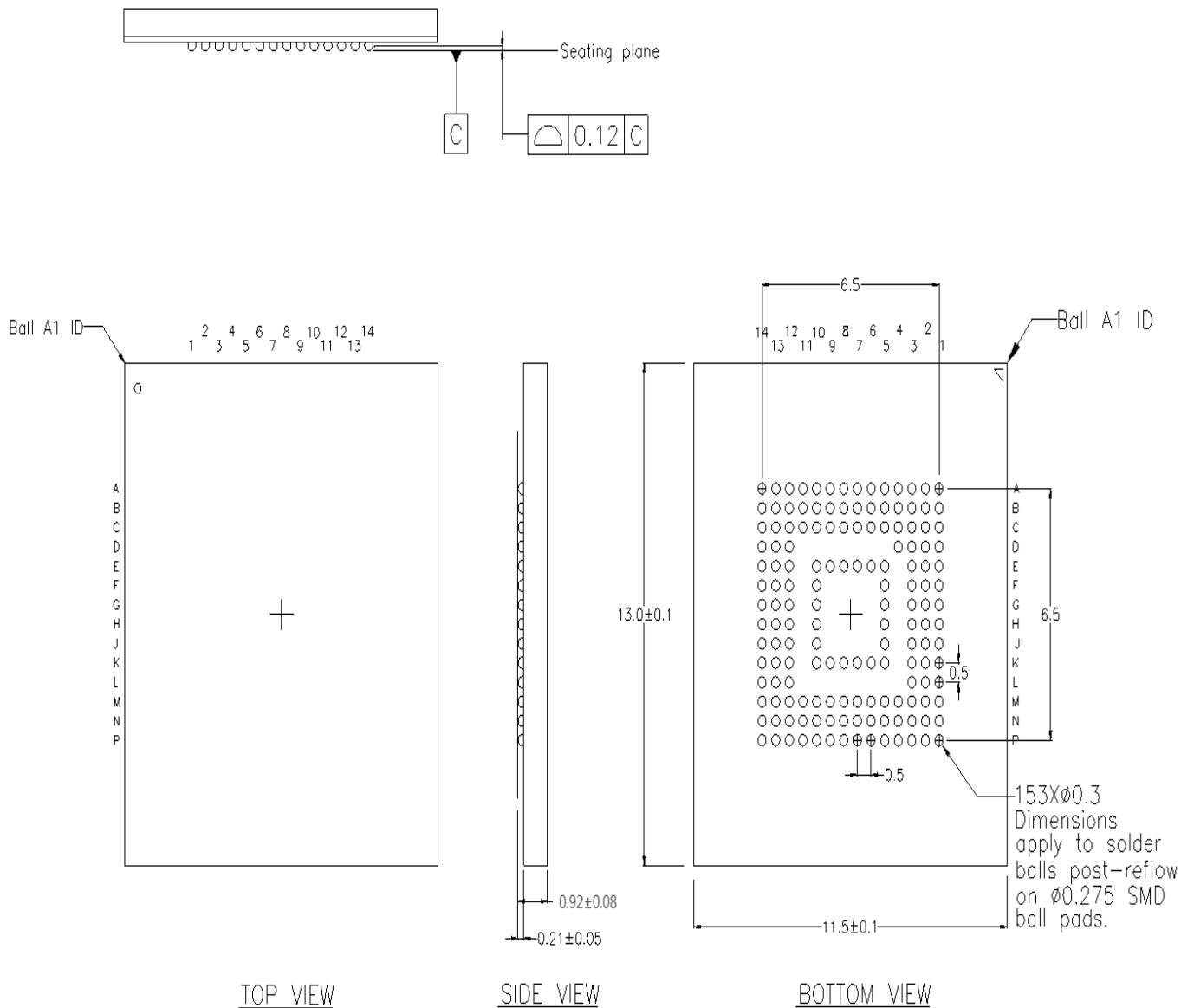


Figure 2. Package Dimension of BGA153

# 3. Product Specification

## 3.1 Performance

Table 3. Performance value in initial stage.

| Mode | Item | Sequential Speed (MB/s) |
| --- | --- | --- |
| | | 128GB |
| HS400 | Write | 251 |
| HS400 | Read | 310 |
| HS200 | Write | 101 |
| HS200 | Read | 170 |
| DDR52 | Write | 80 |
| DDR52 | Read | 83 |

**Note:**

1. Test condition: Under Zbit internal test board, 512KB data transfer, cache on, without OS overhead.

2. Device will exit initial stage and never return to the initial stage again, when the accumulated data size written into different LBAs is greater than the half of device capacity.

## 3.2 Power Consumption

### 3.2.1 Active State

Table 4. Power consumption in active state

| Mode | Operation | Item | Power Consumption (mA) |
| --- | --- | --- | --- |
| | | | 128GB |
| HS400 | Read | $I_{CC}$ | 117 |
| HS400 | Read | $I_{CCQ}$ | 65 |
| HS400 | Write | $I_{CC}$ | 105 |
| HS400 | Write | $I_{CCQ}$ | 49 |
| HS200 | Read | $I_{CC}$ | 95 |
| HS200 | Read | $I_{CCQ}$ | 50 |

| | | | |
|---|---|---|---|
| | Write | $I_{CC}$ | 85 |
| | | $I_{CCQ}$ | 45 |
| DDR52 | Read | $I_{CC}$ | 70 |
| | | $I_{CCQ}$ | 48 |
| | Write | $I_{CC}$ | 68 |
| | | $I_{CCQ}$ | 40 |

**Note:**

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

2. Device operation under 3.3V $V_{CC}$ and 1.8V $V_{CCQ}$.

## 3.2.2 Standby State

Table 5. Power consumption in standby state

| Density | $I_{CCQ}$ (uA) | | $I_{CC}$ (uA) | |
|---|---|---|---|---|
| | 25ºC (Typ.) | 85ºC | 25ºC (Typ.) | 85ºC |
| 128GB | 100 | 470 | 50 | -- |

**Note:**

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

2. In Standby Power mode, VCCQ & VCC power supply is switched on. No data transaction period before entering sleep status, no clock. VCCQ = 1.8V & VCC = 3.3V. Not 100% tested.

## 3.2.3 Sleep State

Table 6. Power consumption in sleep state

| Density | $I_{CCQ}$ (uA) | | $I_{CC}$ (uA) |
|---|---|---|---|
| | 25ºC(Typ.) | 85ºC | |
| 128GB | 100 | 470 | 0 |

**Note:**

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

2. In Sleep state, triggered by CMD5, $V_{CC}$ power supply is switched off ($V_{CCQ}$ on). $V_{CCQ}$ = 1.8V & $V_{CC}$ = 0V. Not 100% tested.

3. In auto power saving mode, NAND power $V_{CC}$ cannot be switched off. However, in sleep mode $V_{CC}$ can be switched off. If NAND power $V_{CC}$ is alive, it is same with that of the Standby state.

## 3.3 Temprature

Table 7. Temperature Range

| Symbol | Min (℃) | Max (℃) |
|---|---|---|
| Operation | -25 | 85 |
| Storage | -40 | 85 |

# 3.4 Partition Size

## 3.4.1 Factory Configuration

The device initially consists of two Boot Partitions, RPMB Partition and User Data Area. Both Boot and RPMB area have fixed size of area and cannot be adjusted.

Table 8. Partition Size

| Density | Boot Partition 1 (KB) | Boot Partition 2 (KB) | RPMB (KB) | User Data Area | |
|---|---|---|---|---|---|
| | | | | Percent | Size (MB) |
| 128GB | 4096 | 4096 | 4096 | 91% | 119,280 |

## 3.4.2 Partition Management

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition with independent address spaces, starting from logical address 0x0000000. Each of the General Purpose Area Partitions and a section of User Data Area partition can be configured as enhanced partition. These partition management operations are one-time programmable.

The enhanced partitions are true SLC mode partition. When customer set some portion as enhanced partitions in User Data Area, these partitions occupy double (MLC)/triple (TLC) size of the original set-up size. If set 1MB for enhanced mode, total 2MB(MLC)/3MB(TLC) user data area is needed to generate 1MB enhanced area.

Table 9. Max Enhanced Partition Size

| Density | Max. Enhanced Partition Size |
|---|---|
| 128GB | 39,760 MB |

# 4. Functional Description

## 4.1 Architecture and Application

The eMMC device consists of a single chip eMMC controller and NAND flash memory. The controller interfaces with a host system allowing data to be written to and read from the NAND flash memory, and handles flash management, including logical to physical translation, bad block management, wear leveling and so on. The interface is only 12-bit line, can support 1-bit/4-bit/8-bit data bus flexibly. Therefore, eMMC host can integrate the eMMC easily, access it like a MMC card, and do not care about NAND flash management.
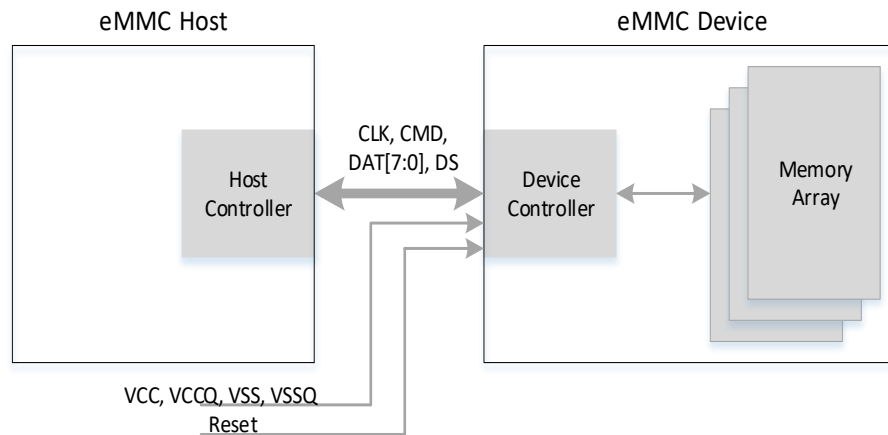


Figure 3. eMMC System Overview

## 4.2 Feature List

The table below lists which common features following JEDEC standards this device supports, and this section introduces several key features of them. For more detailed information about each feature, please refer to JESD84-B51 standard.

Table 10. Supported Feature List

| Feature | Benefit | Support |
|---|---|---|
| Legacy 25/52MHz SDR | | Y |
| 3.3V VCCQ | | Y |
| 1.8V VCCQ | | Y |
| 52MHz DDR | | Y |
| Auto Power Save Mode | | Y |
| Background Operation | Better User Experience (low latency) | Y |

| Feature | Benefit | Support |
|---|---|---|
| Boot Partition and Operation | | Y |
| Boot Partition Individual Write Protection | | Y |
| BKOPS Control | Host control on BKOPs | Y |
| Cache | Better Sequential & Random Writes | Y |
| Cache Barrier | | Y |
| Cache Flush Report | | Y |
| Command Queuing | | Y |
| Context Management | Performance and/or Reliability | Y |
| Configurable Drive Strength | | Y |
| Discard | Improved Performance on Full Media | Y |
| Data Tag | Performance and/or Reliability | Y |
| Data Reliability Definition | Static Data Protection | Y |
| Dynamic Capacity | | Y |
| Device Health Report | Vital NAND info | Y |
| E2MMC | | N |
| Enhanced Strobe | Sync Data out, CRC Response and CMD response between Device and Host in HS400 | Y |
| Enhanced Reliable Write | | Y |
| Extended Partition Attribute | Flexibility | Y |
| Extended Security Protocols | | N |
| Field Firmware Update | | Y |
| FW Configuration Register | | Y |

| Feature | Benefit | Support |
|---|---|---|
| HPI(High Priority Interrupt) | Control Long Reads/Writes | Y |
| HW Reset | Robust System Design | Y |
| HS200 | Speed | Y |
| HS400 | Speed | Y |
| Independent Boot Area Protection | | Y |
| I/O Modification (Overshoot/Undershoot) | | Y |
| Large Sector Size | Potential performance | N |
| Partitioning & Protection | Flexibility | Y |
| Power Off Notification | Faster Boot; Responsiveness | Y |
| Packed Command | Reduce Host Overhead | Y |
| Production State Awareness | Different operation during production | Y |
| Real Time Clock | | Y |
| Reliable Write | | Y |
| RPMB Throughput Improve | Faster RPMB write throughput | Y |
| RPMB | Secure Folders | Y |
| Sanitize | True Wipe | Y |
| Secure Erase | True Wipe | Y |
| Secure TRIM | True Wipe | Y |
| Secure Removal Type | | Y |
| Sleep Mode | | Y |
| Sleep Notification | | Y |

| Feature | Benefit | Support |
|---------|---------|---------|
| Secure Write Protection | Secure Write Protect | Y |
| Thermal Spec. | | Y |
| Trim | | Y |
| VSF Signals | | Y |
| Write Reliability | | Y |

# 4.3 Command Operation

## 4.3.1 Boot Operation

Device supports both boot mode and alternative boot mode. Device supports high speed timing and dual data rate during boot mode.
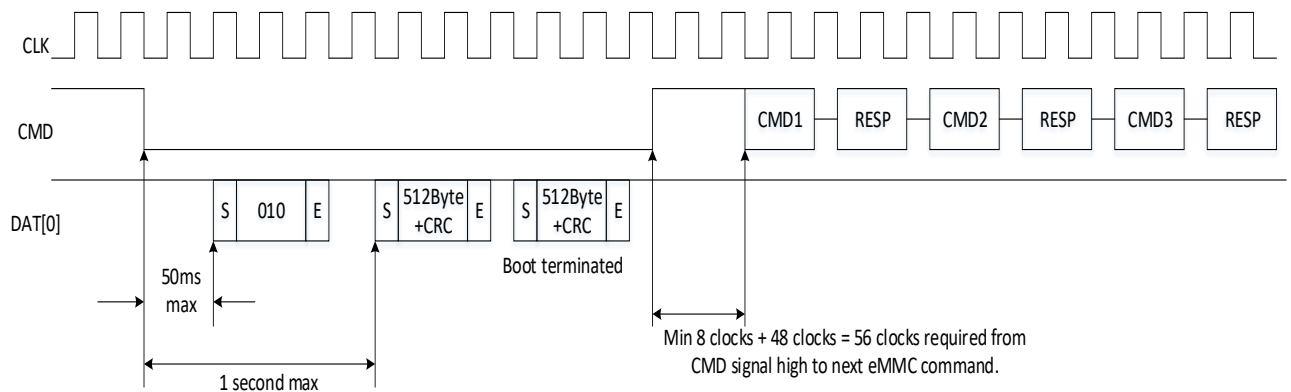


Figure 4. eMMC Boot Mode State Diagram
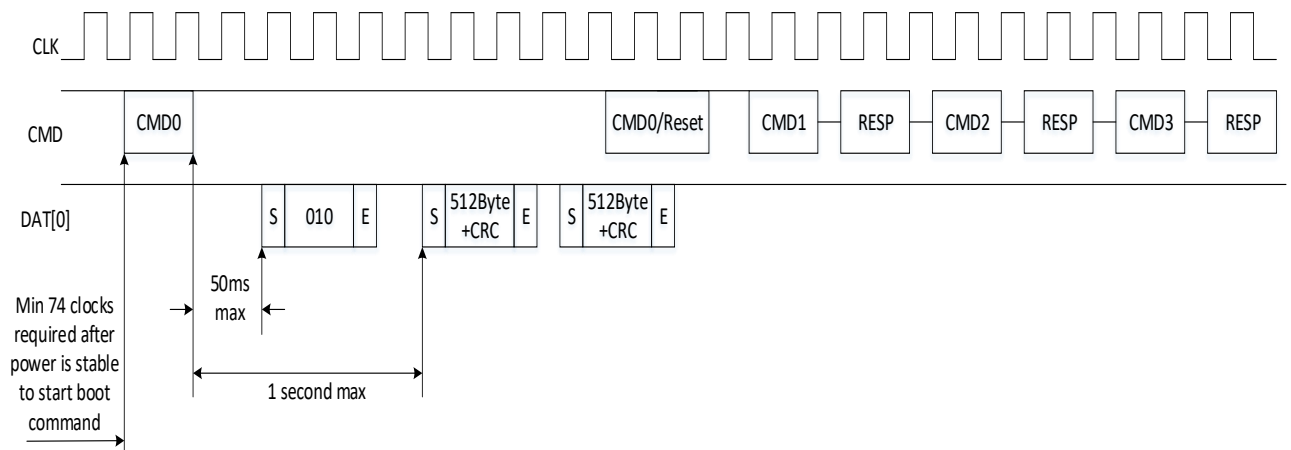


Figure 5. eMMC Alternative Boot Mode State Diagram

Table 11. Timing Parameter

| Timing Parameter | Value |
|---|---|
| (1) Boot ACK Time | < 50 ms |
| (2) Boot Data Time | < 1 s |
| (3) Initialization Time | < 1 s |

## 4.3.2 Partition Management

The device initially consists of two Boot partitions, RPMB partitions and user data area. The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition. For more details, please refer to JESD84-B51 standard.

# 4.4 H/W Reset Operation

H/W reset operation may be used to reset the device, moving the device to a pre-idle state. For more information, refer to JESD84-B51 standard.

# 4.5 Device Health Report

Device supports Device Health Report feature which can provide an estimated indication about the device lifetime that is reflected by the averaged wear out of memory Type A and Type B. It can be queried by standard eMMC command for getting Extended CSD structure. Please refer to below and JEDEC Standards for details.

Table 12. Device Health Report

| Field | EXT_CSD Slice | Description |
|---|---|---|
| DEVICE_LIFE_TIME_EST_TYP_A | 268 | Lifetime estimation of Type A(SLC) area. |
| DEVICE_LIFE_TIME_EST_TYP_B | 269 | Lifetime estimation of Type B(MLC/TLC) area. |
| PRE_EOL_INFO | 267 | Indication about device lifetime reflected by average reserved blocks |

The device health feature will provide a % of the wear of the device in 10% fragments.

# 4.6 Field Firmware Update (FFU)

## 4.6.1 FFU Flow

The feature of Field Firmware Update (FFU) is used to

update the device firmware with an open protocol to users. The host can download a new version of the firmware into the eMMC device by this mechanism and whole FFU process can happen without affecting any user/OS data.

- Field Firmware Update is protected from power interruption events. Any power loss interruption will not corrupt the firmware [device may initialize from next power for either the old or the new firmware).
- Any failure of Field Firmware Update will cause the previous version of firmware to be restored.
- Field Firmware Update supports all bus widths and clocks.
- The binary of Field Firmware Update is protected from invalid firmware Any invalid firmware will cause a Field Firmware Update failure rather than update the device with the wrong firmware.
- The older version of binary cannot be updated with Field Firmware Update To update the device with an older version of firmware, the VSC command, MP Flow, should be issued.

The Zbit eMMC only supports Manual mode (Mode_OPERATION_CODES is not supported). For more details, see as the following chart and register table given below.
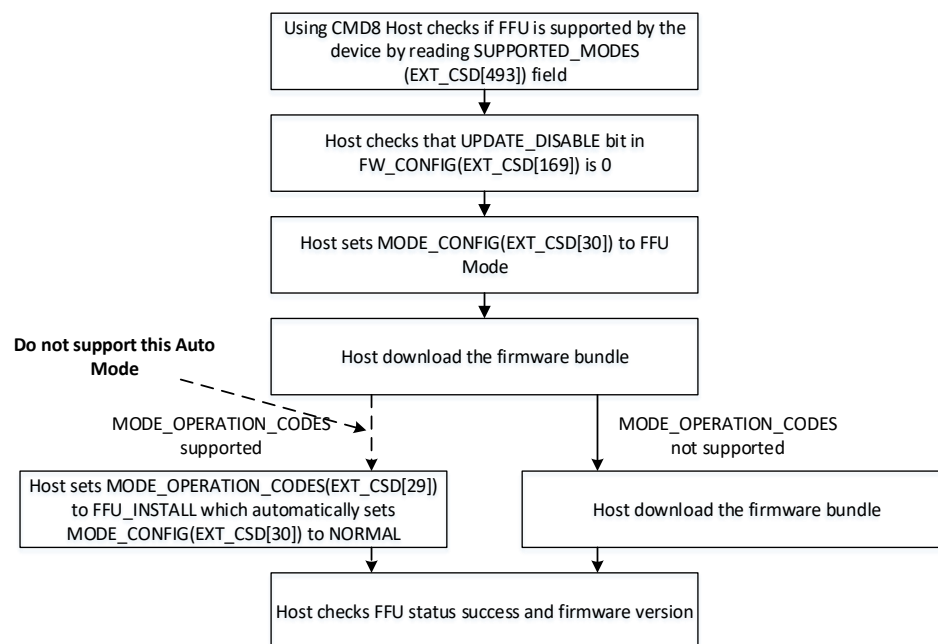


Figure 6. FFU Flow Charter

The Zbit eMMC Field Firmware update command flow:

Table 13. FFU Flow Command

| Operation | Command | Note |
|---|---|---|
| Initialize device to transfer mode | CMD0, ..., CMD7 | |
| Set bus width set frequency | | |
| Set block length to 512B | CMD16<br>Argu: 0x200 | |
| Get FFU argument | CMD8 | |

| Enter FFU mode | CMD6<br>Argu: 0x031E0100 | |
|---|---|---|
| Send Firmware to device | CMD25<br>Argu: FFU_ARGU | |
| Stop data transfer | CMD12<br>Argu: 0x00000000 | |
| Exit FFU mode | CMD6<br>Argu: 0x031E0000 | |
| HW Reset/power cycle | | |
| Re-initialize device to transfer mode | CMD0, CMD1, …, CMD7 | |
| Check if FFU is succeeded | CMD8<br>Argu: 0x00000000 | Check EXT_CSD [26], If FFU_SUCCESS is 0, FFU is succeeded, otherwise FFU is failed. |

## 4.6.2 EXT_CSD Register for FFU

1)   SUPPORTED_MODE [493] (Read Only)

Table 14. EXT_CSD [493]

| Bit | Field | Supportability |
|---|---|---|
| Bit[7:2] | Reserved | - |
| Bit[1] | VSM | Not support |
| Bit[0] | FFU | Supported |

BIT [0]:
   - 0: FFU is not supported by the device.
   - 1: FFU is supported by the device.
BIT [1]:
   - 0: Vendor specific mode (VSM) is not supported by the device.
   - 1: Vendor specific mode is supported by the device

2)   FFU_FEATURE [492] (Read Only)

Table 15. EXT_CSD [492]

| Bit | Field | Supportability |
|---|---|---|
| Bit[7:1] | Reserved | - |
| Bit[0] | SUPPORTED_MODE_OPERATION_CODES | Not support |

BIT[0] :
- 0: Device does not support MODE_OPERATION_CODES field.
- 1: Device supports MODE_OPERATION_CODES field.

3) FFU_ARG [490-487] (Read Only)

Using this field the device reports to the host which value the host should set as an argument for the read and write commands in FFU mode.

4) FFU_CONFIG [169] (R/W)

Table 16. EXT_CSD [169]

| Bit | Field | Supportability |
|---|---|---|
| Bit[7:1] | Reserved | - |
| Bit[0] | Update Disable | Firmware updates enabled (0x0) |

BIT[0] :
- 0: Enable update Firmware.
- 1: Disable update Firmware permanently.

5) FFU_STATUS [26] (R/W/E_P)

Using this field the device reports the status of the FFU process.

Table 17. EXT_CSD [26]

| Value | Description |
|---|---|
| 0x00 | Success |
| 0x01-0x0F | Reserved |
| 0x10 | General Error |
| 0x11 | Firmware Install Error |
| 0x12 | Error in Downloading Firmware |
| Others | Reserved |

6) OPERATION_CODES_TIMEOUT [491] (Read Only)

Maximum timeout for the SWITCH command when setting a value to the MODE_OPERATION_CODES field. The register is set to '0', because the device does not support MODE_OPERATION_CODES.

Table 18. EXT_CSD[491]

| Value | Description |
| --- | --- |
| 0x00 | 0x0 (Not Defined) |
| Others | Reserved |

7) MODE_OPERATION_CODES [29] (W/E_P)

The host sets the operation to be performed at the selected modes, in case MODE_CONFIGS is set to FFU_MODE, MODE_OPERATION_CODES could have the following values. The Zbit device does not support MODE_OPERATION_CODES.

Table 19. EXT_CSD [29]

| Value | Description |
| --- | --- |
| 0x00 | Reserved |
| 0x01 | FFU_INSTALL |
| 0x02 | FFU_ABORT |
| Others | Reserved |

8) MODE_CONFIG [30] (R/W/E_P)

Using this field the host can change the mode of the device.

Table 20. EXT_CSD [30]

| Value | Description |
| --- | --- |
| 0x00 | Normal Mode (To keep the compatibility) |
| 0x01 | FFU Mode |
| 0x02 | Vendor Specific Mode |
| Others | Reserved |

## 4.7 Thermal Spec

This device can enter a Low Power mode when the internal temperature is higher than Upper Bound temperature, while it should come back in Normal Power mode when the internal temperature is lower than Lower Bound temperature. Both thresholds are configurable.

This device may enter the Low Power mode by following means (may or may not be applied to all):

- Device is operated at a lower internal clock: MCU internal bus, NAND flash bus.
- Device intends to add latency between NAND flash operations or host operations.
- Device executes a limited parallelism of NAND flash operations, e.g. limit at only one or two NAND flash for parallelism (not recommended to be implemented as the performance impact may be obvious to the host).
- Other internal device level mechanism at lower power.

When the device is in the Low Power mode it is still transparent to the host for all device functions (e.g. HS400 is still supported). However, the host may be aware of it since the device performance drops in the Low Power model.

## 4.8 Auto Power Save Mode

If the device detects there is no host activities and has no internal operations to do, it shall enter Auto Power Save mode internally after a specific time to reduce power consumption.

- Auto Power Save mode is transparent to the host. The host is not required to send any command to enter or exit Auto Power Save mode.
- Auto Power Save mode ends once the host issues a new command. The device exits Auto Power Save mode automatically with no awareness from the host. However, the 1st new command will be executed after a short latency as the device exits Auto Power Save mode.

## 4.9 Sleep (CMD5)

The Device support using sleep/awake command (CMD5) to switch between a sleep and a standby state. In the sleep state the power consumption of the device is minimized, and the device reacts only to the commands reset command (CMD0) and awake command (CMD5). The VCC power supply support to be switched off in sleep state to minimize power consumption. For more information, refer to JESD84-B51 standard.

## 4.10 Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

## 4.11 Secure Erase/Trim

For backward compatibility reasons, in addition to the standard erase command the eMMC supports the optional Secure Erase command.

- Device may or may not physically erase the data in NAND flash by its own manner.
- Erase /Trim should be issued with Sanitize instead of Secure Erase in the new implementations at system level.

Zbit reserves the right to change specifications without notice.

# 5. Register

Device provides some general and key information of registers: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them can be accessed only corresponding commands. For more details, please refer to JESD84-B51 standard.

- The OCR, CID and CSD registers has information of device and content.
- The RCA and DSR registers are for configuring parameters of device.
- The EXT_CSD register contains both device specific information and actual configuration parameters.

Following sections are for describing all register value of eMMC device at its default. And these values here may be updated in later version without notice.

## 5.1 OCR Register

The 32-bit operation conditions register (OCR) contains: VCC voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finished its power up procedure.

Table 21. OCR Register

| OCR bit | $V_{CCQ}$ Voltage Window | Register Value |
|---------|--------------------------|----------------|
| [6:0]   | Reserved                 | 000 0000b      |
| [7]     | 1.70 ~ 1.95              | 1b             |
| [14:8]  | 2.0 ~ 2.6                | 000 0000b      |
| [23:15] | 2.7 ~ 3.6                | 1 1111 1111b   |
| [28:24] | Reserved                 | 0 0000b        |
| [30:29] | Access Mode              | 10b (sector mode) |
| [31]    | eMMC power up status bit (busy).<br>This bit is set to LOW if the device has not completed the power up routine. | |

## 5.2 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by eMMC protocol. Each device shall have a unique identification number.

Table 22**.** CID Register

| Name | Field | Width | CID-slice | CID Value |
|------|-------|-------|-----------|-----------|
| Manufacturer ID | MID | 8 | [127:120] | 0x5E |
| Reserved | -- | 6 | [119:114] | 0x00 |
| Device/BGA | CBX | 2 | [113:112] | 0x01 |
| OEM/Application ID | OID | 8 | [111:104] | 0x00 |
| Product name | PNM | 48 | [103:56] | 128GB: 0x5A 42 45 4D 41 47 |
| Product revision | PRV | 8 | [55:48] | 0x30 |
| Product serial number | PSN | 32 | [47:16] | -- |
| Manufacturing date | MDT | 8 | [15:8] | -- |
| CRC7 checksum | CRC | 7 | [7:1] | -- |
| not used, always '1' | -- | 1 | [0:0] | -- |

## 5.3 CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27. For more information, refer to JESD84-B51 standard.

Table 23**.** CSD Register

| Name | Field | Width | Type | CSD-slice | Value |
|------|-------|-------|------|-----------|-------|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 0x03 |
| System specification version | SPEC_VERS | 4 | R | [125:122] | 0x04 |
| Reserved | - | 2 | R | [121:120] | 0x00 |
| Data read access-time 1 | TAAC | 8 | R | [119:112] | 0x2F |

| Name | Field | Width | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | 0x01 |
| Max. bus clock frequency | TRAN_SPEED | 8 | R | [103:96] | 0x32 |
| Device command classes | CCC | 12 | R | [95:84] | 0x8F5 |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 0x09 |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 0x00 |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0x00 |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0x00 |
| DSR implemented | DSR_IMP | 1 | R | [76:76] | 0x00 |
| Reserved | - | 2 | R | [75:74] | 0x00 |
| Device size | C_SIZE | 12 | R | [73:62] | 0xFFF |
| Max. read current @ VDD min | VDD_R_CURR_MIN | 3 | R | [61:59] | 0x07 |
| Max. read current @ VDD max | VDD_R_CURR_MAX | 3 | R | [58:56] | 0x07 |
| Max. write current @ VDD min | VDD_W_CURR_MIN | 3 | R | [55:53] | 0x07 |
| Max. write current @ VDD max | VDD_W_CURR_MAX | 3 | R | [52:50] | 0x07 |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | 0x07 |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 0x1F |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 0x1F |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | 0x0F |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 0x01 |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | 0x00 |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 0x03 |

| Name | Field | Width | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 0x09 |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0x00 |
| Reserved | - | 4 | R | [20:17] | 0x00 |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] | 0x00 |
| File format group | FILE_FORMAT_GRP | 1 | R/W | [15:15] | 0x00 |
| Copy flag (OTP) | COPY | 1 | R/W | [14:14] | 0x00 |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] | 0x00 |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0x00 |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | 0x00 |
| ECC code | ECC | 2 | R/W/E | [9:8] | 0x00 |
| CRC | CRC | 7 | R/W/E | [7:1] | |
| Not used, always'1' | - | 1 | — | [0:0] | |

**Note:**

    1. Register type explanations:

      (1) R = Read-only.

      (2) R/W = One-time programmable and readable.

      (3) R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.

    2. Reserved bits should be read as 0.

# 5.4 Extended CSD Register

The Device-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E below) can be changed by CMD27. The type of the CSD Registry entries below is coded as follows:

Table 24. Extended CSD Register

| Name | Field | Size | Type | CSD-slice | Value |
|------|-------|------|------|-----------|-------|
| Reserved | - | 6 | TBD | [511:506] | 0x00 |
| Extended Security Command Error | EXT_SECURITY_ERR | 1 | R | [505] | 0x00 |
| Supported Command Set | S_CMD_SET | 1 | R | [504] | 0x01 |
| HPI features | HPI_FEATURES | 1 | R | [503] | 0x01 |
| Background operation support | BKOPS_SUPPORT | 1 | R | [502] | 0x01 |
| Max packed read commands | MAX_PACKED_READS | 1 | R | [501] | 0x3F |
| Max packed write commands | MAX_PACKED_WRITES | 1 | R | [500] | 0x3F |
| Data Tag Support | DATA_TAG_SUPPORT | 1 | R | [499] | 0x01 |
| Tag Unit Size | TAG_UNIT_SIZE | 1 | R | [498] | 0x00 |
| Tag Resource Size | TAG_RES_SIZE | 1 | R | [497] | 0x00 |
| Context management capabilities | CONTEXT_CAPABILITIES | 1 | R | [496] | 0x05 |
| Large Unit size | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 0x07 |
| Extended partitions attribute support | EXT_SUPPORT | 1 | R | [494] | 0x03 |
| Supported modes | SUPPORTED_MODES | 1 | R | [493] | 0x01 |
| FFU features | FFU_FEATURES | 1 | R | [492] | 0x00 |
| Operation codes timeout | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 0x00 |
| FFU Argument | FFU_ARG | 4 | R | [490:487] | 0xFFFFFF5F |
| Barrier support | BARRIER_SUPPORT | 1 | R | [486] | 0x00 |
| Reserved | | 177 | TBD | [485:309] | 0x00 |
| CMD Queuing Support | CMDQ_SUPPORT | 1 | R | [308] | 0x01 |
| CMD Queuing Depth | CMDQ_DEPTH | 1 | R | [307] | 0x1F |

Zbit reserves the right to change specifications without notice.

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Reserved | | 1 | | [306] | 0x00 |
| Number of FW sectors correctly programed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4 | R | [305:302] | 0x00 |
| Vendor proprietary health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 32 | R | [301:270] | 0x00 |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | R | [269] | 0x01 |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | R | [268] | 0x01 |
| Pre EOL information | PRE_EOL_INFO | 1 | R | [267] | 0x01 |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | R | [266] | 0x40 |
| Optimal write size | OPTIMAL_WRITE_SIZE | 1 | R | [265] | 0x40 |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 0x07 |
| Device version | DEVICE_VERSION | 2 | R | [263:262] | - |
| Firmware version | FIRMWARE_VERSION | 8 | R | [261:254] | - |
| Power class for 200MHz, DDR at VCC=3.6 | PWR_CL_DDR_200_360 | 1 | R | [253] | 0xDD |
| Cache size | CACHE_SIZE | 4 | R | [252:249] | 0x00000400 |
| Generic CMD6 timeout | GENERIC_CMD6_TIME | 1 | R | [248] | 0x64 |
| Power off notification (long) timeout | POWER_OFF_LONG_TIME | 1 | R | [247] | 0x8C |
| Background operation status | BKOPS_STATUS | 1 | R | [246] | 0x00 |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | R | [245:242] | 0x00 |
| 1st initialization time after partitioning | INI_TIMEOUT_AP | 1 | R | [241] | 0x0A |
| Cache Flushing Policy | CACHE_FLUSH_POLICY | 1 | R | [240] | 0x01 |
| Power class for 52MHz, DDR at VCC=3.6V | PWR_CL_DDR_52_360 | 1 | R | [239] | 0xAA |

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Power class for 52MHz, DDR at VCC=1.95V | PWR_CL_DDR_52_195 | 1 | R | [238] | 0xDD |
| Power class for 200MHz at VCCQ=1.95V, VCC=3.6V | PWR_CL_200_195 | 1 | R | [237] | 0xDD |
| Power class for 200MHz at VCCQ=1.3V, VCC=3.6V | PWR_CL_200_130 | 1 | R | [236] | 0xDD |
| Minimum Write Performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 0x00 |
| Minimum Read Performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 0x00 |
| Reserved | | 1 | TBD | [233] | 0x00 |
| TRIM Multiplier | TRIM_MULT | 1 | R | [232] | 0x5 |
| Secure Feature support | SEC_FEATURE_SUPPORT | 1 | R | [231] | 0x55 |
| Secure Erase Multiplier | SEC_ERASE_MULT | 1 | R | [230] | 0x08 |
| Secure TRIM Multiplier | SEC_TRIM_MULT | 1 | R | [229] | 0x08 |
| Boot information | BOOT_INF | 1 | R | [228] | 0x07 |
| Reserved | | 1 | TBD | [227] | 0x00 |
| Boot partition size | BOOT_SIZE_MULT | 1 | R | [226] | 0x20 |
| Access size | ACC_SIZE | 1 | R | [225] | 0x07 |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 0x01 |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | 1 | R | [223] | 0x5 |
| Reliable write sector count | REL_WR_SEC_C | 1 | R | [222] | 0x01 |
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | R | [221] | 0x10 |
| Sleep current (Vcc) | S_C_VCC | 1 | R | [220] | 0x08 |
| Sleep current (VccQ) | S_C_VCCQ | 1 | R | [219] | 0x08 |

Zbit reserves the right to change specifications without notice.

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Production state awareness timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 0x0A |
| Sleep/awake timeout | S_A_TIMEOUT | 1 | R | [217] | 0x17 |
| Sleep Notification Timeout | SLEEP_NOTIFICATIN_TIME | 1 | R | [216] | 0x11 |
| Sector Count | SEC_COUNT | 4 | R | [215:212] | 0x0E8F8000 |
| Secure Write Protect Information | SECURE_WP_INFO | 1 | R | [211] | 0x01 |
| Minimum Write Performance for 8bit at 52MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 0x0A |
| Minimum Read Performance for 8bit at 52MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 0x0A |
| Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 0x0A |
| Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 0x0A |
| Minimum Write Performance for 4bit at 26MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 0x0A |
| Minimum Read Performance for 4bit at 26MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 0x0A |
| Reserved | | 1 | TBD | [204] | 0x00 |
| Power class for 26MHz at 3.6V 1 R | PWR_CL_26_360 | 1 | R | [203] | 0x22 |
| Power class for 52MHz at 3.6V 1 R | PWR_CL_52_360 | 1 | R | [202] | 0xAA |
| Power class for 26MHz at 1.95V 1 R | PWR_CL_26_195 | 1 | R | [201] | 0x22 |
| Power class for 52MHz at 1.95V 1 R | PWR_CL_52_195 | 1 | R | [200] | 0xAA |
| Partition switching timing | PARTITION_SWITCH_TIME | 1 | R | [199] | 0x32 |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | 0x0A |
| I/O Driver Strength | DRIVER_STRENGTH | 1 | R | [197] | 0x1F |
| Device type | DEVICE TYPE | 1 | R | [196] | 0x57 |

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Reserved | | 1 | TBD | [195] | 0x00 |
| CSD STRUCTURE | CSD_STRUCTURE | 1 | R | [194] | 0x02 |
| Reserved | | 1 | TBD | [193] | 0x00 |
| Extended CSD revision | EXT_CSD_REV | 1 | R | [192] | 0x08 |
| Command set | CMD_SET | 1 | R/W/E_P | [191] | 0x00 |
| Reserved | | 1 | TBD | [190] | 0x00 |
| Command set revision | CMD_SER_REV | 1 | R | [189] | 0x00 |
| Reserved | | 1 | TBD | [188] | 0x00 |
| Power class | POWER_CLASS | 1 | R/W/E_P | [187] | 0x00 |
| Reserved | | 1 | TBD | [186] | 0x00 |
| High-speed interface timing | HS_TIMING | 1 | R/W/E_P | [185] | 0x00 |
| Strobe Support | STROBE_SUPPORT | 1 | R | [184] | 0x01 |
| Bus width mode | BUS_WIDTH | 1 | W/E_P | [183] | 0x00 |
| Reserved | | 1 | TBD | [182] | 0x00 |
| Erased memory content | ERASED_MENM_CONT | 1 | R | [181] | 0x00 |
| Reserved | | 1 | TBD | [180] | 0x00 |
| Partition configuration | PARTITION_CONFIG | 1 | R/W/E & R/W/E_P | [179] | 0x00 |
| Boot config protection | BOOT_CONFIG_PROT | 1 | R/W & R/W/C_P | [178] | 0x00 |
| Boot bus Conditions | BOOT_BUS_CONDITIONS | 1 | R/W/E | [177] | 0x00 |
| Reserved | | 1 | TBD | [176] | 0x00 |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E_P | [175] | 0x00 |

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Boot write protection status registers | BOOT_WP_STATUS | 1 | R | [174] | 0x00 |
| Boot area write protection register | BOOT_WP | 1 | R/W & R/W/C_P | [173] | 0x00 |
| Reserved | | 1 | TBD | [172] | 0x00 |
| User area write protection register | USER_WP | 1 | R/W, R/W/C_P & R/W/E_P | [171] | 0x00 |
| Reserved | | 1 | TBD | [170] | 0x00 |
| FW configuration | FW_CONFIG | 1 | R/W | [169] | 0x00 |
| RPMB Size | RPMB_SIZE_MULT | 1 | R | [168] | 0x20 |
| Write reliability setting register | WR_REL_SET | 1 | R/W | [167] | 0x1F |
| Write reliability parameter register | WR_REL_PARAM | 1 | R | [166] | 0x15 |
| Start Sanitize operation | SANITIZE_START | 1 | W/E_P | [165] | 0x00 |
| Manually start background operations | BKOPS_START | 1 | W/E_P | [164] | 0x00 |
| Enable background operations handshake | BKOPS_EN | 1 | R/W & R/W/E | [163] | 0x00 |
| H/W reset function | RST_n_FUNCTION | 1 | R/W | [162] | 0x00 |
| HPI management | HPI_MGMT | 1 | R/W/E_P | [161] | 0x00 |
| Partitioning Support | PARTITIONING_SUPPORT | 1 | R | [160] | 0x07 |
| Max Enhanced Area Size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | 0x00136A |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 0x00 |
| Partitioning Setting | PARTITION_SETTING_COMPLETED | 1 | R/W | [155] | 0x00 |
| General Purpose Partition Size | GP_SIZE_MULT | 12 | R/W | [154:143] | 0x00 |
| Enhanced User Data Area Size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 0x00 |

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Enhanced User Data Start Address | ENH_START_ADDR | 4 | R/W | [139:136] | 0x00 |
| Reserved | | 1 | TBD | [135] | 0x00 |
| Bad Block Management mode | SEC_BAD_BLK_MGMNT | 1 | R/W | [134] | 0x00 |
| Production state awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 0x00 |
| Package Case Temperature is controlled | TCASE_SUPPORT | 1 | W/E_P | [132] | 0x00 |
| Periodic Wake-up | PERIODIC_WAKEUP | 1 | R/W/E | [131] | 0x00 |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 0x00 |
| Reserved | | 2 | TBD | [129:128] | 0x00 |
| Vendor Specific Fields | VENDOR_SPECIFIC_FIELD | 64 | vendor or specific | [127:64] | - |
| Native sector size | USE_NATIVE_SECTOR | 1 | R | [63] | 0x00 |
| Sector size emulation | NATIVE_SECTOR_SIZE | 1 | R/W | [62] | 0x00 |
| Sector size | DATA_SECTOR_SIZE | 1 | R | [61] | 0x00 |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | 1 | R | [60] | 0x00 |
| Class 6 commands control | CLASS_6_CTRL | 1 | R/W/E_P | [59] | 0x00 |
| number of addressed group to be Released | DYNCAP_NEEDED | 1 | R | [58] | 0x00 |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 0x00 |
| Exception events status | EXCEPTION_EVENTS_STATUS | 2 | R | [55:54] | 0x00 |
| Extended Partitions Attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 0x00 |
| Context configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 0x00 |
| Packed command status | PACKED_COMMAND_STATUS | 1 | R | [36] | 0x00 |

| Name | Field | Size | Type | CSD-slice | Value |
|---|---|---|---|---|---|
| Packed command failure index | PACKED_FAILU RE_INDEX | 1 | R | [35] | 0x00 |
| Power Off Notification | POWER_OFF_NO TIFICATION | 1 | R/W/E_P | [34] | 0x00 |
| Control to turn the Cache ON/OFF | CACHE_CTRL | 1 | R/W/E_P | [33] | 0x00 |
| Flushing of the cache | FLUSH_CACHE | 1 | W/E_P | [32] | 0x00 |
| Control to turn the Barrier ON/OFF | BARRIER_CTRL | 1 | R/W | [31] | 0x00 |
| Mode config | MODE_CONFIG | 1 | R/W/E_P | [30] | 0x00 |
| Mode operation codes | MODE_OPERATI ON_CODES | 1 | W/E_P | [29] | 0x00 |
| Reserved | | 2 | TBD | [28:27] | 0x00 |
| FFU status | FFU_STATUS | 1 | R | [26] | 0x00 |
| Pre loading data size | PRE_LOADING_ DATA_SIZE | 4 | R/W/E_P | [25:22] | 0x00 |
| Max pre loading data size | MAX_PRE_LOAD ING_DATA_SIZE | 4 | R | [21:18] | 0x4DA8000 |
| Product state awareness enablement | PRODUCT_STAT E_AWARENESS_ ENABLEMENT | 1 | R/W/E & R | [17] | 0x01 |
| Secure Removal Type | SECURE_REMOV AL_TYPE | 1 | R/W & R | [16] | 0x39 |
| Command Queue Mode Enable | CMDQ_MODE_E N | 1 | R/W/E_P | [15] | 0x00 |
| Reserved | | 15 | TBD | [14:0] | 0x00 |

**Note:**
1. Register type explanations:
   1) R = Read-only.
   2) R/W = One-time programmable and readable.
   3) R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
   4) R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable.
   5) R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
   6) W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable.
2. Reserved bits should be read as 0.

## 5.5 RCA Register

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

## 5.6 DSR Register

The16-bit DSR register can be optionally used to improve the bus performance for extended operating conditions depending on parameters like bus length, transfer rate or the number of devices. The CSD register carries the information of the DSR register usage. The default value of the DSR register is 0x404.

# 6. Electrical Characteristics

## 6.1 Supply Voltage

Table 25. Supply Voltage

| Item | Min (V) | Max (V) |
|------|---------|---------|
| VCCQ | 1.7 | 1.95 |
|      | 2.7 | 3.6 |
| VCC | 2.7 | 3.6 |
| VSS | -0.5 | 0.5 |

## 6.2 Bus Signal Line Load

The total capacitance $C_L$ of each line of the eMMC bus is the sum of the bus master capacitance $C_{HOST}$, the bus capacitance $C_{BUS}$ itself and the capacitance $C_{DEVICE}$ of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 26. Bus Signal Line Load

| Parameter | Symbol | Min | Typ. | Max | Unit | Remark |
|-----------|--------|-----|------|-----|------|--------|
| Pull-up resistance for CMD | $R_{CMD}$ | 4.7 | | 100 | KΩ | to prevent bus floating |
| Pull-up resistance for DAT0-DAT7 | $R_{DAT}$ | 10 | | 100 | KΩ | to prevent bus floating |

| Internal pull up resistance DAT1-DAT7 | $R_{int}$ | 10 | | 150 | KΩ | to prevent unconnected lines floating |
|---|---|---|---|---|---|---|
| Single Device capacitance | $C_{DEVICE}$ | | | 30 | pF | |
| Maximum signal line inductance | | | | 16 | nH | fPP <= 52 MHz |

Table 27. Capacitance and Resistance for HS400 mode

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Bus signal line capacitance | $C_L$ | | | 13 | pF | Single Device |
| Single Device capacitance | $C_{DEVICE}$ | | | 6 | pF | |
| Pull-down resistance for Data Strobe | $R_{Data\ Strobe}$ | 10 | | 100 | KΩ | |

# 6.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



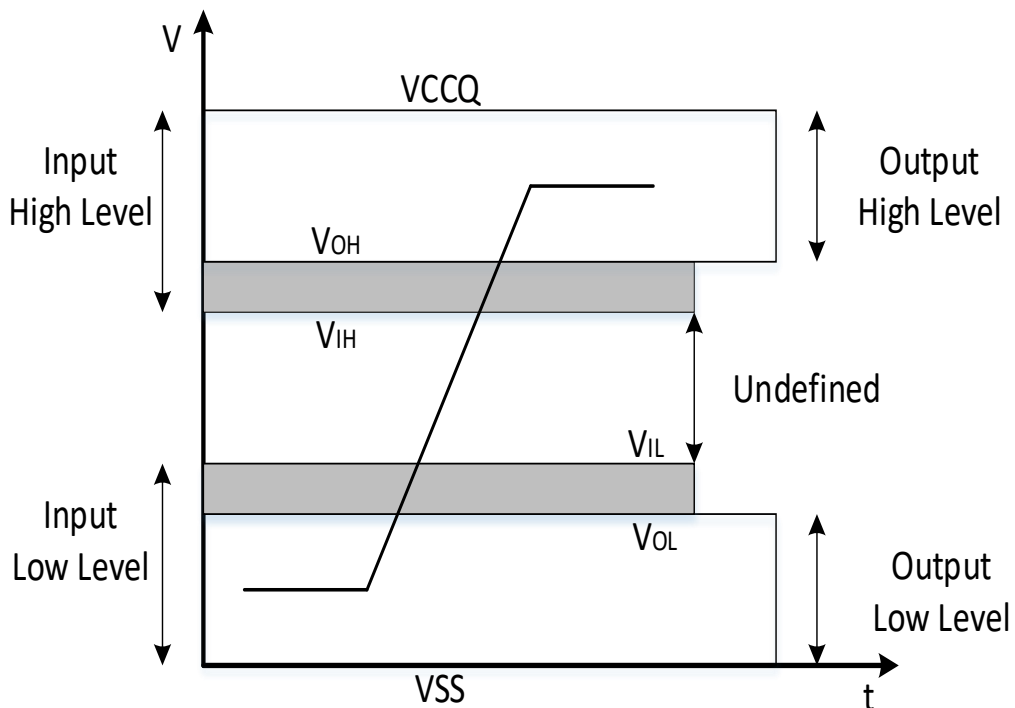Figure 7. Bus Signal Levels

Table 28. Bus Signal Levels

| Parameter | Symbol | Min (V) | Max (V) | Remark |
|-----------|--------|---------|---------|--------|
| **Open-drain mode** | | | | |
| Output HIGH voltage | $V_{OH}$ | $V_{CCQ}$ - 0.2 | - | (1) |
| Output LOW voltage | $V_{OL}$ | - | 0.3 | |
| **Push-pull mode (VCCQ: 2.7V - 3.6V)** | | | | |
| Output HIGH voltage | $V_{OH}$ | 0.75 * $V_{CCQ}$ | - | IOH = -100uA @ VCCQ min |
| Output LOW voltage | $V_{OL}$ | - | 0.125 * $V_{CCQ}$ | IOL = 100uA @ VCCQ min |
| Input HIGH voltage | $V_{IH}$ | 0.625 * $V_{CCQ}$ | $V_{CCQ}$ + 0.3 | - |
| Input LOW voltage | $V_{IL}$ | VSS - 0.3 | 0.25 * $V_{CCQ}$ | - |
| **Push-pull mode (VCCQ: 1.70V - 1.95V)** | | | | |
| Output HIGH voltage | $V_{OH}$ | VCCQ - 0.45 | - | IOH = -2mA |
| Output LOW voltage | $V_{OL}$ | - | 0.45 | IOL = 2mA |
| Input HIGH voltage | $V_{IH}$ | 0.65 * VCCQ | VCCQ + 0.3 | (2) |
| Input LOW voltage | $V_{IL}$ | VSS - 0.3 | 0.35 * VCCQ | (3) |

**NOTE:**
1) Because VOH depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet VOH Min value.
2) 0.7 x VCCQ for MMC4.3 and older revisions.
3) 0.3 x VCCQ for MMC4.3 and older revisions.

# 6.4 Bus Timing Specification

The Zbit eMMC follows JEDEC standard, for timing specification of all bus mode, including High Speed SDR, High Speed DDR, HS200, HS400, please refer to JESD84-B51 standard.
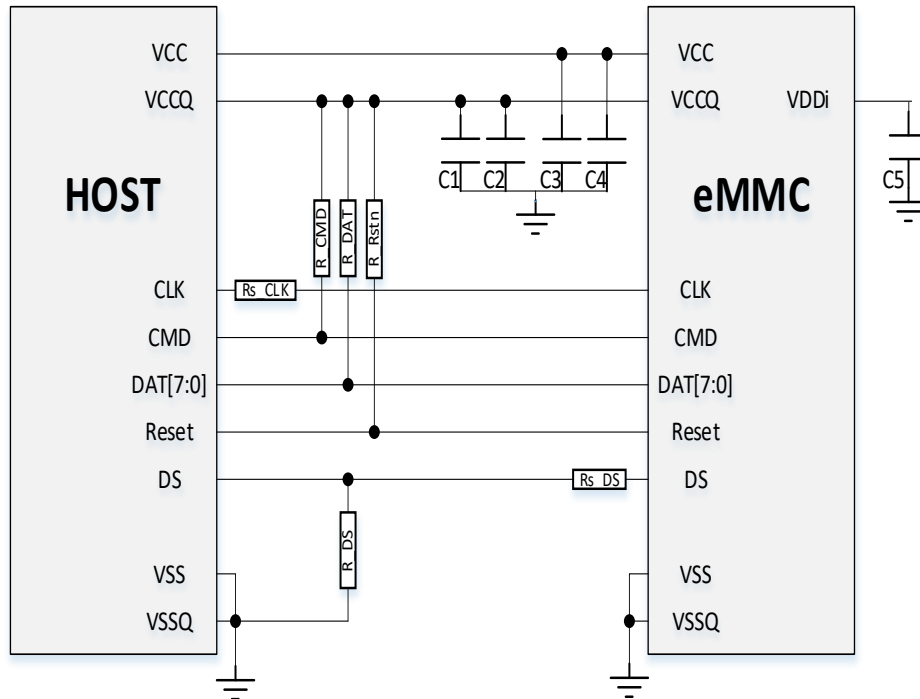
# 7. Design Guide

## 7.1 Connect Guide



Figure 8. eMMC Connect Guide

## 7.2 Component Recommendation

Table 29. Component recommendation

| Description | Symbol | Min. | Max. | Typ. | Note |
|---|---|---|---|---|---|
| Pull-up resistance for CMD (KΩ) | R_CMD | 4.7 | 100 | 10 | Pull-up resistance should be put on CMD line to prevent bus floating. |
| Pull-up resistance for DAT0~7 (KΩ) | R_DAT | 10 | 100 | 50 | Pull-up resistance should be put on DAT line to prevent bus floating. |
| Data strobe(DS) (KΩ) | R_DS | 10 | 100 | 10 | Pull-down resistance should be put on DS line to prevent bus floating. |
| Serial resistance on DS (Ω) | Rs_DS | 0 | 30 | 0 | To reduce overshooting/undershooting Note: If the host uses HS400, we recommend removing this resister for better DS signal. |

| Description | Symbol | Min. | Max. | Typ. | Note |
|---|---|---|---|---|---|
| Pull-up resistance for Rstn (KΩ) | R_Rstn | 10 | 100 | 50 | It is not necessary to put pull-up resistance on Rstn line if host does not use H/W reset. (Extended CSD register [162] = 0b) |
| Serial resistance on CLK (Ω) | Rs_CLK | 0 | 30 | 0 | To reduce overshooting/undershooting Note: If the host uses HS200/HS400, we recommend removing this resister for better CLK signal. |
| VCCQ capacitor value (uF) | C1 | 1 | 10 | 2.2 | Coupling capacitor should be connected with VCCQ and VSSQ as closely as possible. |
| | C2 | 0.1 | 0.22 | 0.1 | |
| VCC capacitor value (uF) | C3 | 1 | 10 | 2.2 | Coupling capacitor should be connected with VCC and VSS as closely as possible. |
| | C4 | 0.1 | 0.22 | 0.1 | |
| VDDI capacitor value (uF) | C5 | 0 | 0.1 | 0 | No capacitor is recommended. Coupling capacitor should be connected with VDDI and VSSQ as closely as possible. |
| CLK/CMD/DS/DAT [7:0] impedance (Ω) | | 45 | 55 | 50 | For impedance match. |