

4-channel × 75W, Digital Input Class-D Automotive Audio Amplifier with Advanced diagnostics, 2MHz Switching Frequency and High Resolution Bandwidth

1. Features

- AEC-Q100 for Automotive Applications
 - Temperature Grade 1: -40°C to +125°C T_A
- Input Voltage Range: 4.5V to 26.4V
- Battery Load Dump Compatible: 40V
- Low R_{ds(ON)}=75mΩ for High Efficiency
- Audio Outputs
 - Four-channels Bridge-tied Load (BTL)
 - Two-channel Parallel BTL (PBTL)
 - 45W, 10% THD into 2Ω at 14.4V BTL
 - 25W, 10% THD into 4Ω at 14.4V BTL
 - 75W, 10% THD into 4Ω at 24V BTL
- 2MHz Switching PWM for Reduced Size and Cost of Output L-C Filter
- Audio Performance into 4Ω at 14.4V BTL
 - THD+N <0.01% at 1W
 - 40μV_{RMS} Output Noise
- Load Diagnostics
 - DC Load Diagnostics: Open Load, Short Load, Short to PVDD, Short to GND
 - Line output Detection up to 18kΩ
 - AC Load Diagnostic: Impedance and Phase Report
 - Real-time Load Diagnostics: Open Load, Short Load
- Low EMI technology
 - Multi-device PWM Phase Synchronization
 - Spread Spectrum and Smart Edge Rate Control, Channel to Channel PWM Phase Optimization
 - EMC Compliance According to CISPR25
- 8 Levels Thermal Warning Report
- Output Clipping Detection with Programmable Threshold and Latched or Non-latched Warning Report
- Cycle-by-cycle Current Limit with Programmable Threshold and Time Window
- Protections

- Over Current Protection
- Over Voltage and Under Voltage Protection
- Over Temperature Protection
- Speaker DC Protection

2. Applications

- Automotive Head Unit
- Automotive External Amplifier

3. General Description

The ACM9634-Q1 device is a four-channel high-efficient class-D amplifier with digital input, low EMI output stages. A 2MHz PWM switching frequency enabling a cost-optimized solution in a very small PCB size.

The ACM9634-Q1 supports start-stop cranking down to 4.5V and compatible with 40V load dump.

The ACM9634-Q1 supports 16/24/32-bit data, I²S-Bus, and TDM with 4/8/16 slots per frame. High resolution bandwidth supports up to 20kHz (I²S 48kHz), 40kHz (I²S 96kHz) and 80kHz (I²S 192kHz).

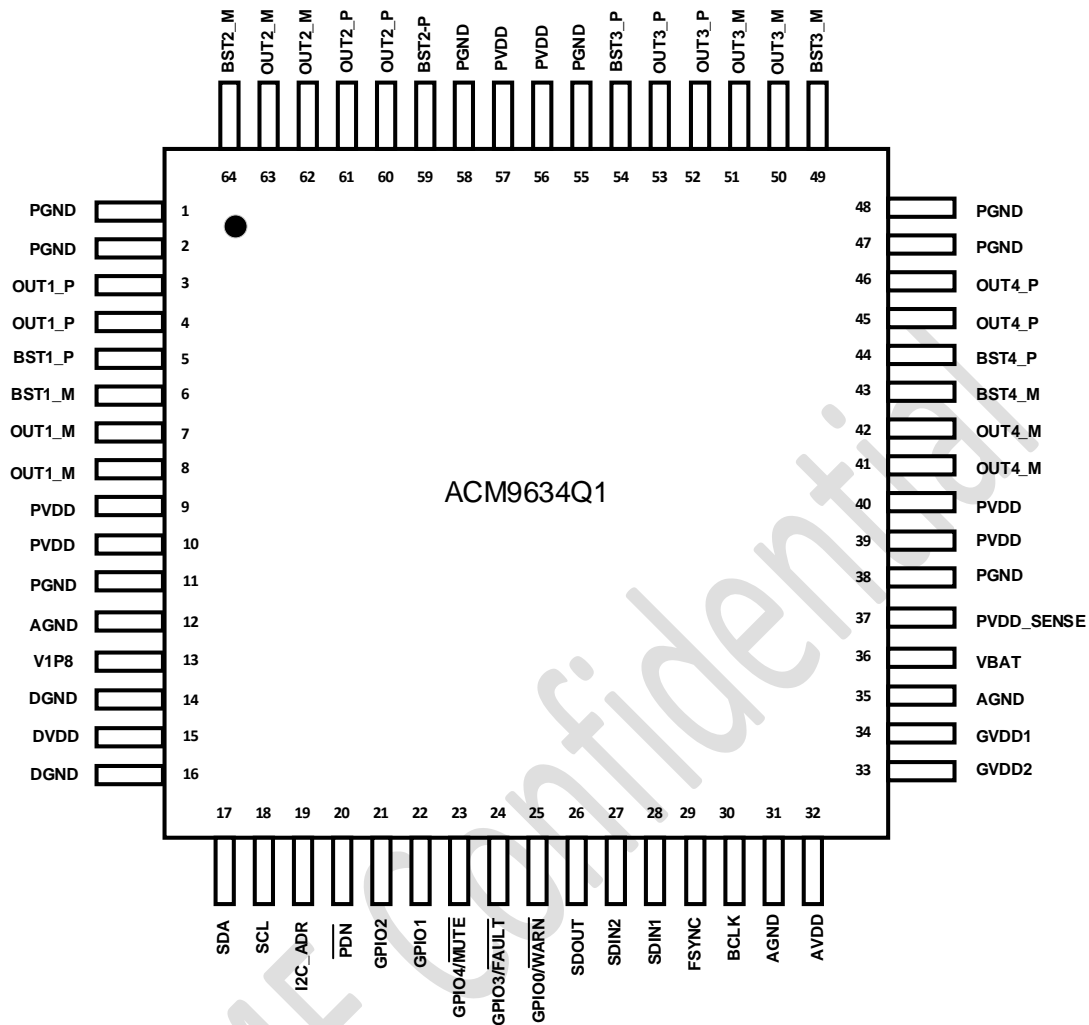
The ACM9634-Q1 device supports advanced load diagnostics for speaker DC load diagnostic, AC Load diagnostic and real-time load diagnostics. The ACM9634-Q1 device integrates various protection features to protect the device, speaker, and system against fault events, such as short circuit protection, over temperature protection, speaker DC protection, battery load dump protection, over/under voltage protection, clock error protection.

The device is offered in a very compact and thin LQFP 10mm × 10mm package.

4. Device Information

Part number	Package	Body size
ACM9634	LQFP-64	10 mm × 10 mm

5. Pin Configuration and Function Descriptions



Pin No.	Name	Type	Description
52,53	OUT3_P	Positive Output	Positive Output for Channel 3
9,10,39,40,56,57	PVDD	Power	PVDD Voltage Input
41,42	OUT4_M	Negative Output	Negative Output for Channel 4
43	BST4_M	Power	Bootstrap Capacitor Connection for High Side Gate Driver
1,2,11,38,47,48,55,58	PGND	Ground	Ground for Power FETs
44	BST4_P	Power	Bootstrap Capacitor Connection for High Side Gate Driver
45,46	OUT4_P	Positive Output	Positive Output for Channel 4
37	PVDD_SENSE	Power	Connect to PVDD for Device Internal PVDD sense
36	VBAT	Power	Battery Voltage Input
12,31,35	AGND	Ground	Ground for Analog Circuits
34	GVDD1	Power	Gate Driver Voltage Regulator Output for Channel 1 and Channel 2, Connect 1 μ F Capacitor to AGND
33	GVDD2	Power	Gate Driver Voltage Regulator Output for Channel 3 and Channel 4, Connect 1 μ F Capacitor to AGND
32	AVDD	Power	Internal Regulator Output for Internal Analog Circuit, Connect 1 μ F Capacitor to AGND
30	BCLK	Digital Input	Bit Clock for Digital Serial Bus
29	FSYNC	Digital Input	Frame Clock (LRCLK) for Digital Serial Bus
28	SDIN1	Digital Input	I ² S Data Input (Channel 1 and Channel 2) for Digital Serial Bus, or TDM Data Input
27	SDIN2	Digital Input	I ² S Data Input (Channel 3 and Channel 4) for Digital Serial Bus

26	SDOUT	Digital In/Out	Default as Data Output. General Purpose I/O, can be Configured as Other Function
25	GPI00_WARN	Digital In/Out	Default as Warning (Clipping Warning, OT Warning) Indicator. General Purpose I/O, can be Configured as Other Function.
15	DVDD	Power	Power Supply for Digital IO (3.3V or 1.8V).
24	GPI03/FAULT	Digital In/Out	Default as Fault Report. General Purpose I/O, can be Configured to Other Function.
23	GPI04/MUTE	Digital In/Out	Default As MUTE Function. General Purpose I/O, can be Configured to Other Function.
14,16	DGND	Ground	Ground for Digital.
13	V1P8	Power	Regulator Output for Internal Digital Core Voltage (1.8V Output), Connect 1 μ F Capacitor to DGND.
22	GPI01	Digital In/Out	Default as OFF. General Purpose I/O, can be Configured to Other Function.
21	GPI02	Digital In/Out	Default as OFF. General Purpose I/O, can be Configured to Other Function.
20	$\overline{\text{PDN}}$	Digital In	Power Down Enable. Low=Power Down. High=Enable.
19	I2C_ADR	Analog In	I ² C Device Address. 6 Different Pull Up/Down Resistor Support 6 Different I ² C Device Address.
18	SCL	Digital In	I ² C Clock.
17	SDA	Digital In/Out	I ² C Data.
7,8	OUT1_M	Negative Output	Negative Output for Channel 1.
6	BST1_M	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
3,4	OUT1_P	Positive Output	Positive Output for Channel 1.
5	BST1_P	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
62,63	OUT2_M	Negative Output	Negative Output for Channel 2.
64	BST2_M	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
59	BST2_P	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
60,61	OUT2_P	Positive Output	Positive Output for Channel 2.
50,51	OUT3_M	Negative Output	Negative Output for Channel 3.
49	BST3_M	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
54	BST3_P	Power	Bootstrap Capacitor Connection for High Side Gate Driver.
Thermal Pad	-	GND	Provides Both Electrical and Thermal Connection for the Device. Heatsink Must be Connected to GND.

6. Specifications

6.1 Absolute Maximum Ratings

Operating with ambient temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
PVDD, VBAT	Analog Power supply voltage relative to GND		-0.3	30	V
V _{MAX}	Transient supply voltage: PVDD, VBAT	t≤100ms	-0.3	40	V
V _{VDD}	Digital Power supply voltage relative to GND		-0.3	3.5	V
V _{LOGIC}	Input voltage for logic pins (SCL, SDA, SDIN1, SDIN2, BLCK, FSYNC, SDOOUT, GPIO0~4)		-0.3	V _{DVDD_IO} +0.5	V
I _{MAX}	Maximum current per pin-PVDD, VBAT, OUTxP, OUTxM, GND	Peak Audio Current, t < 25ms		8	A
T _J	Maximum operating junction temperature range		-55	175	°C
T _{stg}	Storage temperature range		-55	150	°C

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	+/- 2000
		Charged-device model (CDM), per AEC Q100-011	All pins	+/-750
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 16, 17, 32, 33, 48, 49 and 64)	+/- 750

(1) AEC Q100-002 indicates that HBM stressing should be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD	Output FET Supply Voltage Range	Relative to GND	4.5	14.4	26.4	V
VBAT	Battery Supply Voltage Range	Relative to GND	4.5	14.4	18	V
DVDD	Digital Logic Supply	Relative to GND	1.62	3.3	3.5	V
T _A	Ambient temperature		-40		125	V
T _J	Junction temperature	An adequate thermal design is required	-40		160	°C
R _L	Nominal speaker load impedance	BTL mode, (4.5V<PVDD≤14.4V)	1.6	4		Ω
		BTL mode, (4.5V<PVDD≤26.4V)	3.2	4		
		PBTL mode	1.6	2		

6.4 Thermal Information

THERMAL METRIC		LQFP 64	°C/W
		64 PINS	
R _{θJC(top)}	Junction-to-top case thermal resistance, measured at the center on the top of the package ⁽¹⁾	1.26	

(1) Top cold plate as per JEDEC best practice guidelines (JESD51) in contact with package top side (E-pad). Ambient temperature set to 85°C.

6.5 Electrical Characteristics

Test Condition: Ambient temperature = 25°C, PVDD = VBAT =14.4V, VDD=3.3V, $R_L = 4\Omega$, $P_{OUT} = 1W/ch$, $f_{IN}=1kHz$, $F_{SW}=2MHz$, AES17 FILTER, LC filter = 3.3 μ H+1 μ F, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OPERATING CURRENT						
I_{IDLE}	PVDD + VBAT idle current	All channels playing, no audio input		106	mA	
I_{SD}	PVDD + VBAT shutdown current	Shutdown active, $V_{DVDD_IO} = 0V$		5	μ A	
I_{DVDD}	DVDD supply current	All channels playing, -60dBFS signal		24	mA	
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4 Ω , PVDD=14.4V, THD+N=1%, Case Temperature = 75°C	22	24	W	
		4 Ω , PVDD=14.4V, THD+N=10%, Case Temperature = 75°C	26	28	W	
		4 Ω , PVDD=24V, 384kHz F_{SW} , THD+N =1%, Case Temperature = 75°C	56	61	W	
		4 Ω , PVDD=24V, 384kHz F_{SW} , THD+N =10%, Case Temperature = 75°C	72	77	W	
		2 Ω , PVDD=14.4V, THD+N=1%, Case Temperature = 75°C	38	41	W	
		2 Ω , PVDD=14.4V, THD+N=10%, Case Temperature = 75°C	43	47	W	
Efficiency	Power Efficiency	4 \times 25W output power, 4 Ω load, case temperature = 25°C		90%		
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	25°C, including bond wire and package resistance		75	m Ω	
$R_{DS(on)}$	FET drain-to-source resistance	25°C, not including bond wire and package resistance		60	m Ω	
AUDIO PERFORMANCE						
V_n	Output noise voltage	Zero input, A-weighting, PVDD=14.4V, System Gain = 29.5V _p /FS		40	μ V _{rms}	
GAIN	Peak Output Voltage at 0dBFS input	Register Configurable	5.24	29.5	V _p /FS	
G_{ERROR}	Channel-to-channel gain variation		-0.5	0	0.5	dB
PSRR	Power-supply rejection ratio	PVDD = 14.4V _{dc} + 1V _{RMS} , f =1kHz		-90		dB
THD+N	Total harmonic distortion + noise	$P_{out} = 1W$, Load = 4 Ω , PVDD=14.4V		0.02		%
OVERVOLTAGE (OV) PROTECTION						
V_{PVDD_OV}	PVDD overvoltage protection threshold		27	28	29	V
$V_{PVDD_OV_HYS}$	PVDD overvoltage recovery hysteresis			0.5		V
V_{VBAT_OV}	VBAT overvoltage protection threshold		27	28	29	V
$V_{VBAT_OV_HYS}$	VBAT overvoltage recovery hysteresis			0.5		V
UNDERVOLTAGE (UV) PROTECTION						
$PVDD_{UV}$	PVDD undervoltage shutdown		3.7		4.5	V
$PVDD_{UV_HYS}$	PVDD undervoltage recovery hysteresis			0.3		V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT _{UV}	VBAT undervoltage shutdown		3.7		4.5	V
VBAT _{UV,HYS}	VBAT undervoltage recovery hysteresis			0.3		V
OVERTEMPERATURE (OT) PROTECTION						
OTW _{CHANNEL}	Channel over temperature warning for each channel	OTW warning code = 000		155		°C
		OTW warning code = 001		145		
		OTW warning code = 010		135		
		OTW warning code = 011		125		
		OTW warning code = 100		115		
		OTW warning code = 101		105		
		OTW warning code = 110		95		
OTW _{GLOBAL}	Global junction over temperature warning	OTW warning code = 000		155		°C
		OTW warning code = 001		145		
		OTW warning code = 010		135		
		OTW warning code = 011		125		
		OTW warning code = 100		115		
		OTW warning code = 101		105		
		OTW warning code = 110		95		
OTSD _{CHANNEL}	Channel over temperature shutdown	Register configurable		175		°C
OTSD _{GLOBAL}	Global junction over temperature shutdown			160		°C
OT _{HYS}	Over temperature hysteresis			15		°C
OVER CURRENT PROTECTION						
I _{CBC,THRES}	Cycle-by-cycle current limit level, percentage to over current shutdown threshold	CBC Level 1		40		%
		CBC Level 2		50		
		CBC Level 3		60		
		CBC Level 4		70		
		CBC Level 5		80		
		CBC Level 6		90		
DC DETECT						
DC _{DETECT}	Output DC detection threshold			2		V
DIGITAL INPUT PINS						
V _{IH}	Input logic level high		70			%V _{DVDD}
V _{IL}	Input logic level low				30	%V _{DVDD}
I _{IH}	Input logic current, high	V _i = DVDD			15	μA
I _{IL}	Input logic current, low	V _i = 0			15	μA
DIGITAL OUTPUT PINS						
V _{OH}	Output voltage for logic level high		90			%V _{DVDD}
V _{OL}	Output voltage for logic level low				10	%V _{DVDD}
LOAD DIAGNOSTICS						
S2G	Maximum resistance to detect a short from OUT pins to GND	Register configurable			200	Ω
S2P	Maximum resistance to detect a short from OUT pins to PVDD	Register configurable			1000	Ω
SL	Shorted load detection	Short load Threshold register			+/-	Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	tolerance	adjustable, 0.5Ω - 5Ω			0.5	
OL	Open Load			87		Ω
T _{DC_DIAG}	DC diagnostic time	4 Channels run simultaneously, no load fault, with default setting			240	ms
LO	Maximum detectable impedance for line output mode	Register configurable		12		kΩ
T _{LINE_DIAG}	Line output diagnostic time	No load fault		150		ms
AC _{IMP_ACC}	AC impedance accuracy	Stimulus frequency = 19kHz, R _L = 4Ω, Impedance at output pins		+/-0.5		Ω
T _{AC_DIAG}	AC diagnostic time	4 channels run simultaneously, with default setting		100		ms
F _{AC}	AC diagnostic test frequency	Register configurable	0.1		24	kHz

6.6 Timing Requirements

Test Condition: Ambient temperature = 25°C, PVDD = VBAT = 14.4V, VDD=3.3V, R_L = 4Ω, P_{OUT} = 1W/ch, f_{IN}=1kHz, F_{sw}=2MHz, AES17 FILTER, LC filter = 3.3μH+1μF, unless otherwise noted.

6.7 Function Block Diagram

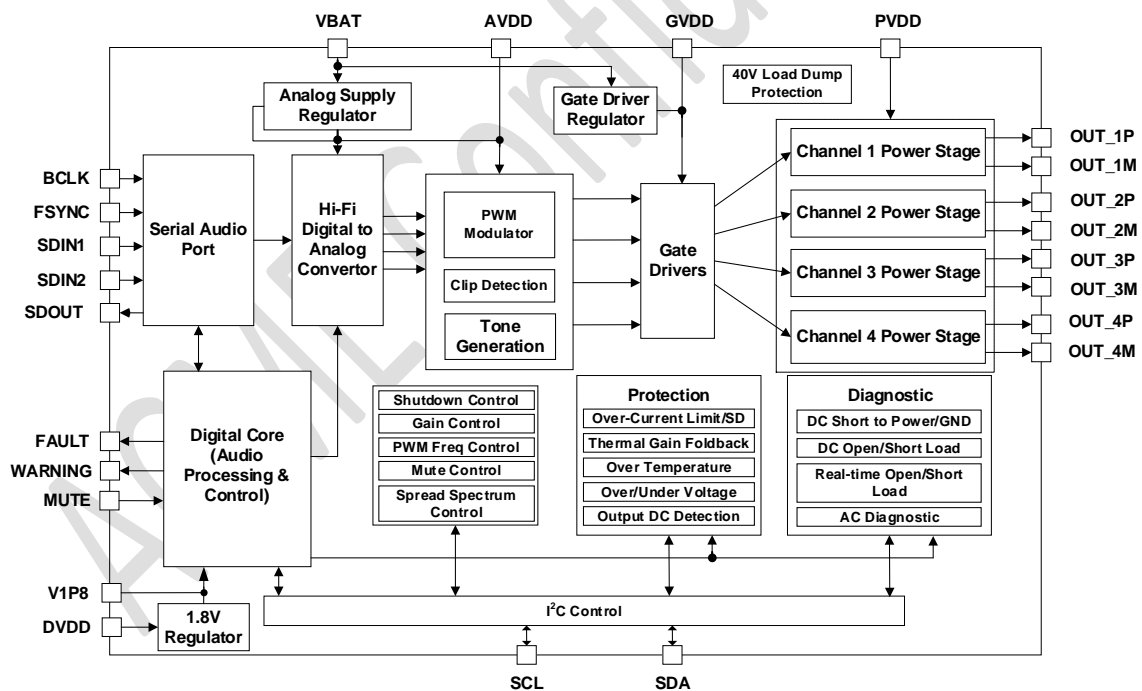


Figure 6-1. Function Block Diagram

6.8 Typical Characteristics

6.8.1 14.4V, Bridge-Tied Load (BTL)

Test Condition: Ambient temperature = 25°C, PVDD = VBAT = 14.4V, VDD=3.3V, $R_L = 4\Omega$, $P_{OUT} = 1W/ch$, $f_{IN}=1kHz$,

$F_{sw}=2MHz$, AES17 FILTER. LC filter = $3.3\mu H+1\mu F$ for 2MHz F_{sw} and $10\mu H+1\mu F$ for 384kHz, unless otherwise noted.

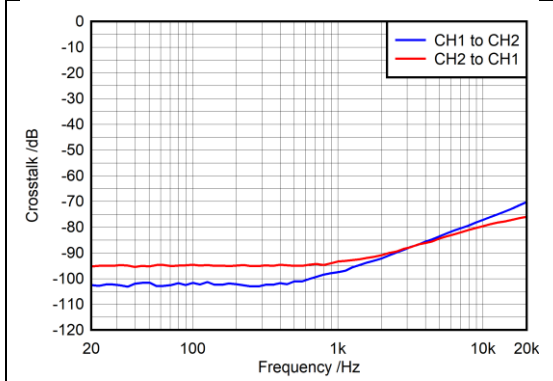


Figure 6-2. Crosstalk vs. Frequency

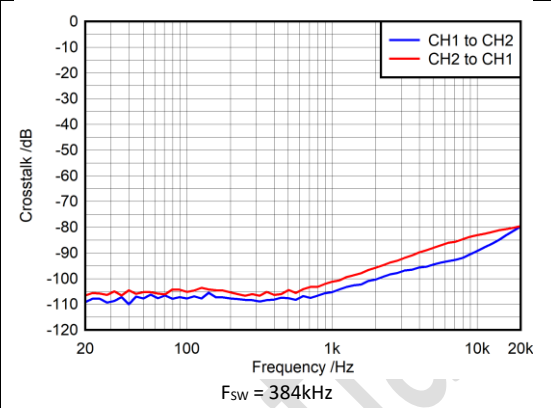


Figure 6-3. Crosstalk vs. Frequency

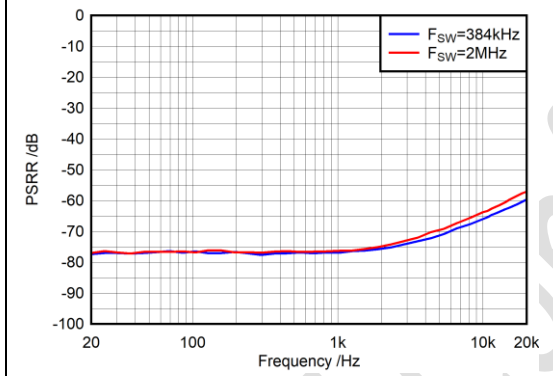


Figure 6-4. PSRR vs. PVDD

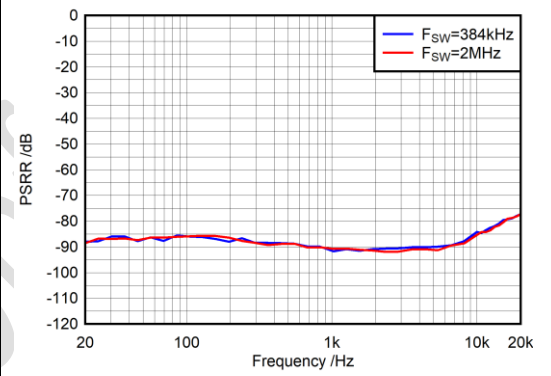


Figure 6-5. PSRR vs. VBAT

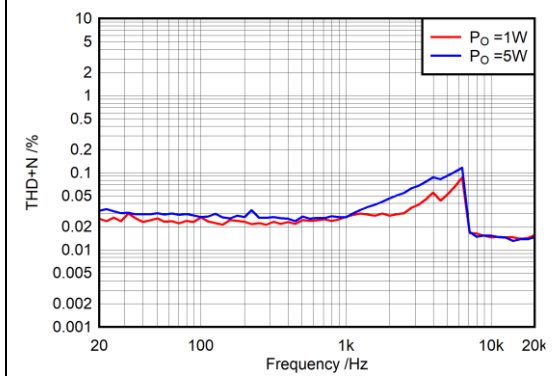


Figure 6-6. THD+N vs. Frequency

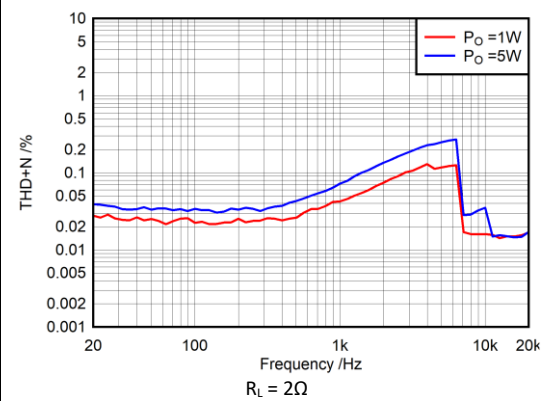


Figure 6-7. THD+N vs. Frequency

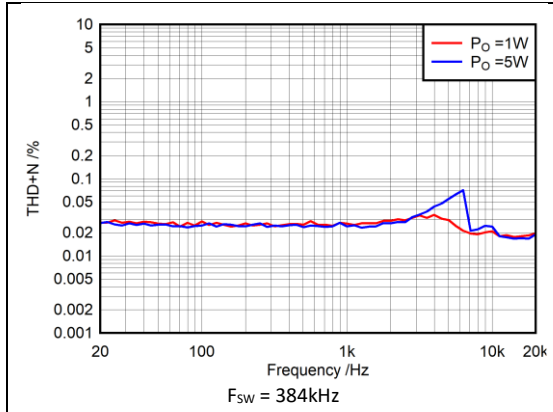


Figure 6-8. THD+N vs. Frequency

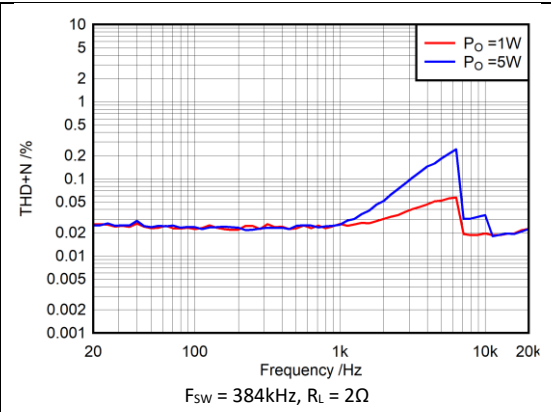


Figure 6-9. THD+N vs. Frequency

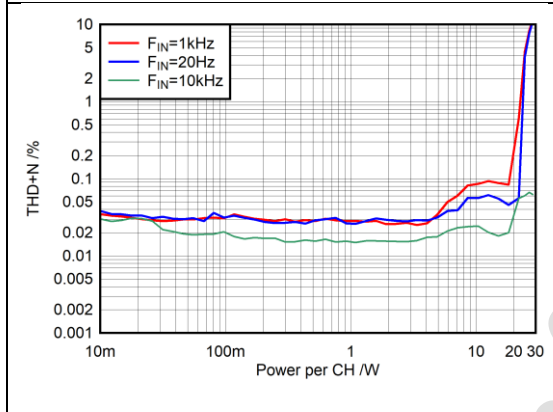


Figure 6-10. THD+N vs. Power

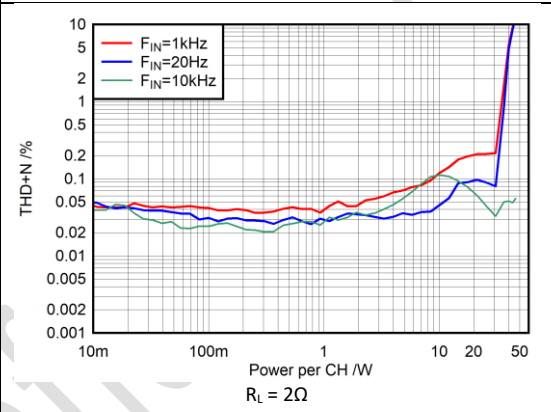


Figure 6-11. THD+N vs. Power

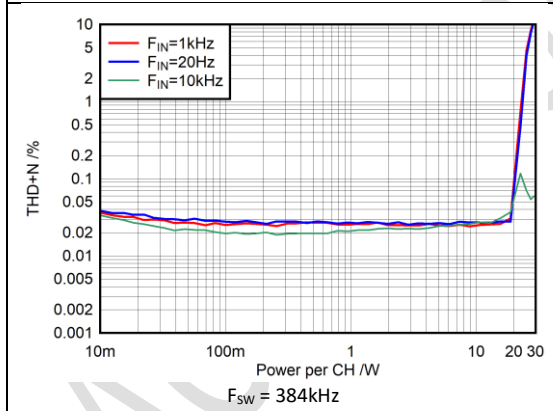


Figure 6-12. THD+N vs. Power

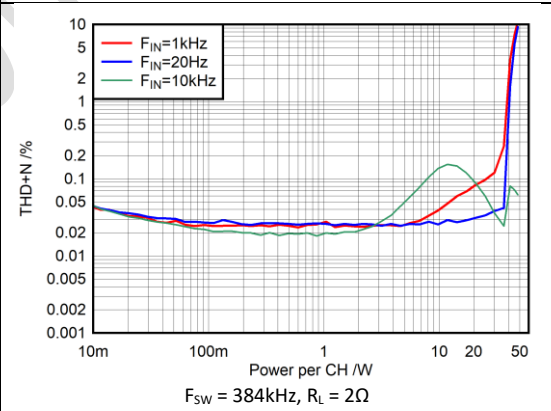


Figure 6-13. THD+N vs. Power

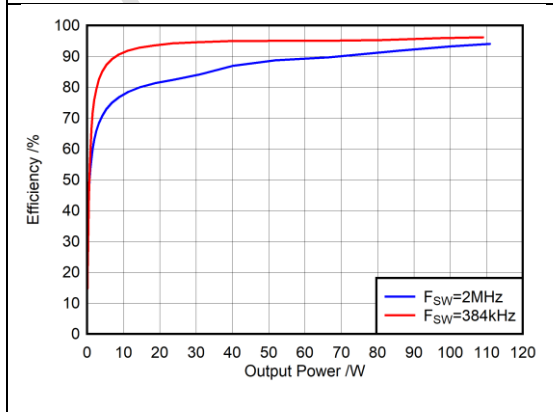


Figure 6-14. Efficiency

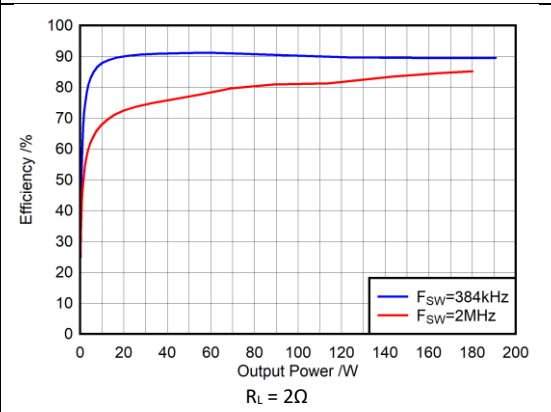


Figure 6-15. Efficiency

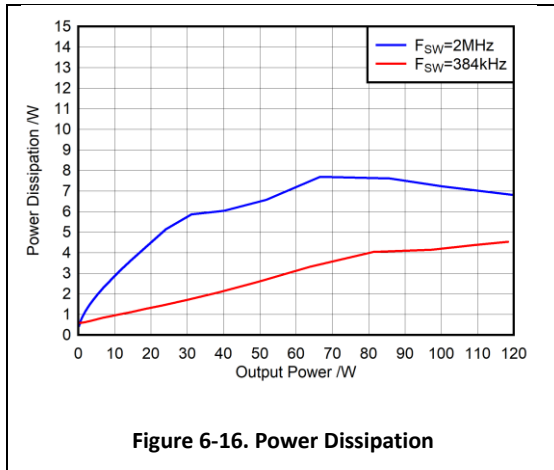


Figure 6-16. Power Dissipation

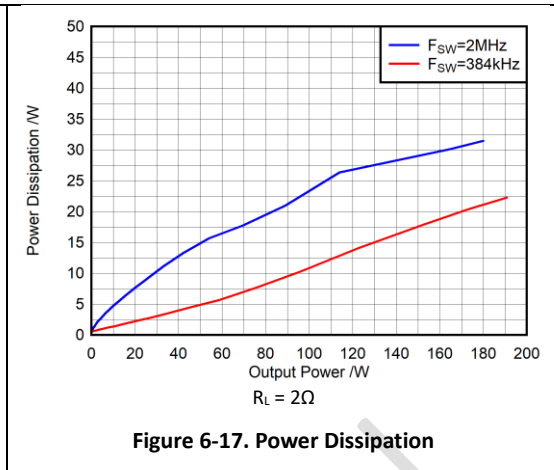


Figure 6-17. Power Dissipation

6.8.2 24V, Bridge-Tied Load (BTL)

Test Condition: Ambient temperature = 25°C, PVDD=24V, VBAT=14.4V VDD=3.3V, $R_L = 4\Omega$, $P_{OUT} = 1\text{W}/\text{ch}$, $f_{IN}=1\text{kHz}$,

$F_{sw}=384\text{kHz}$, AES17 FILTER, LC filter = $10\mu\text{H}+1\mu\text{F}$ for 384kHz F_{sw} , unless otherwise noted.

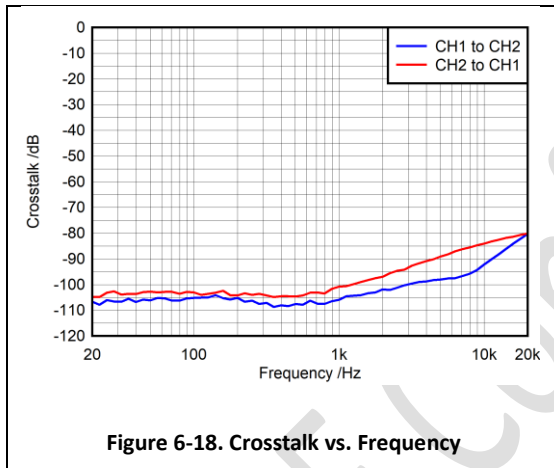


Figure 6-18. Crosstalk vs. Frequency

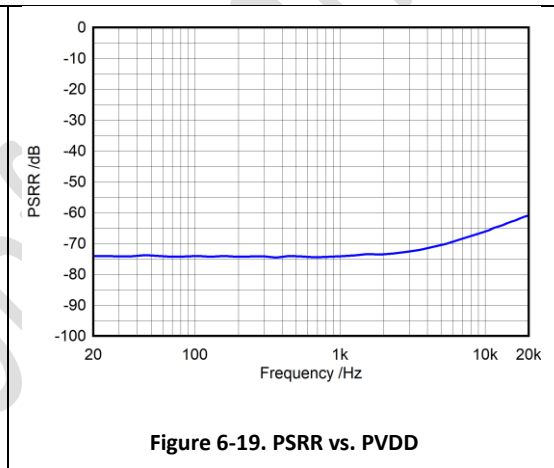


Figure 6-19. PSRR vs. PVDD

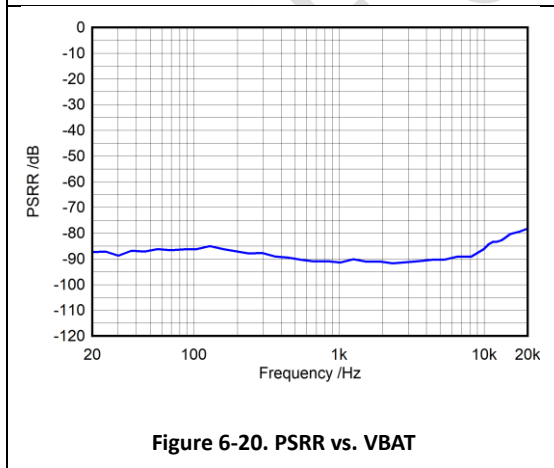


Figure 6-20. PSRR vs. VBAT

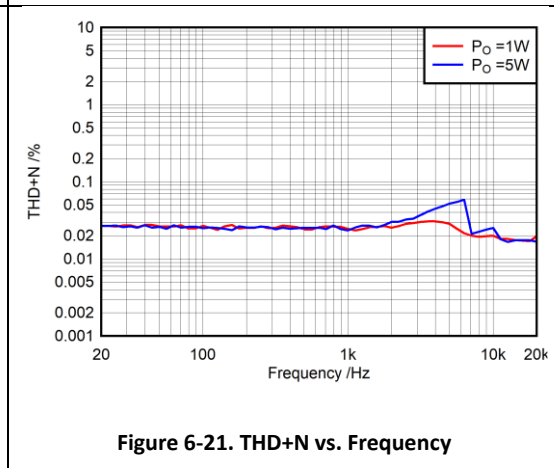
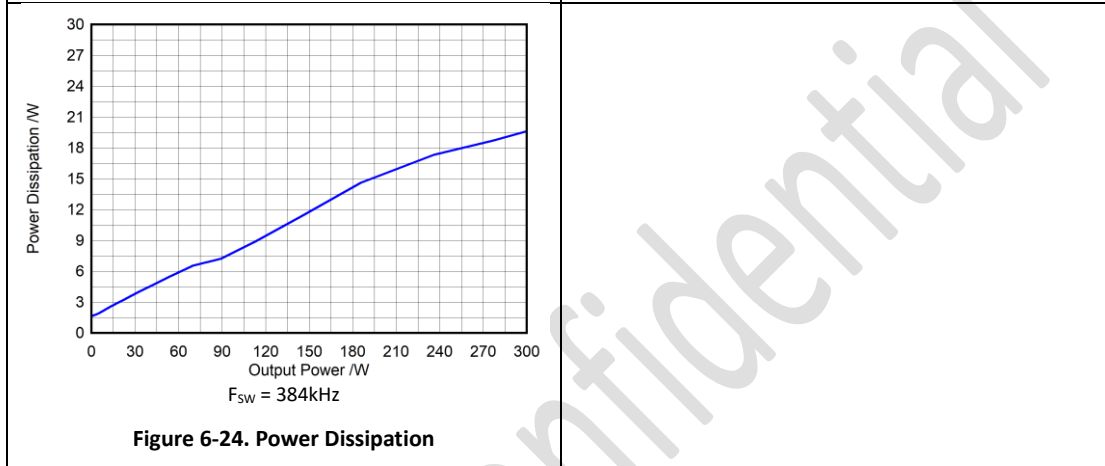
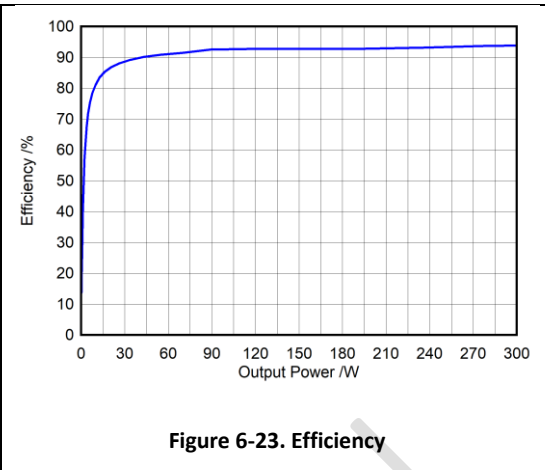
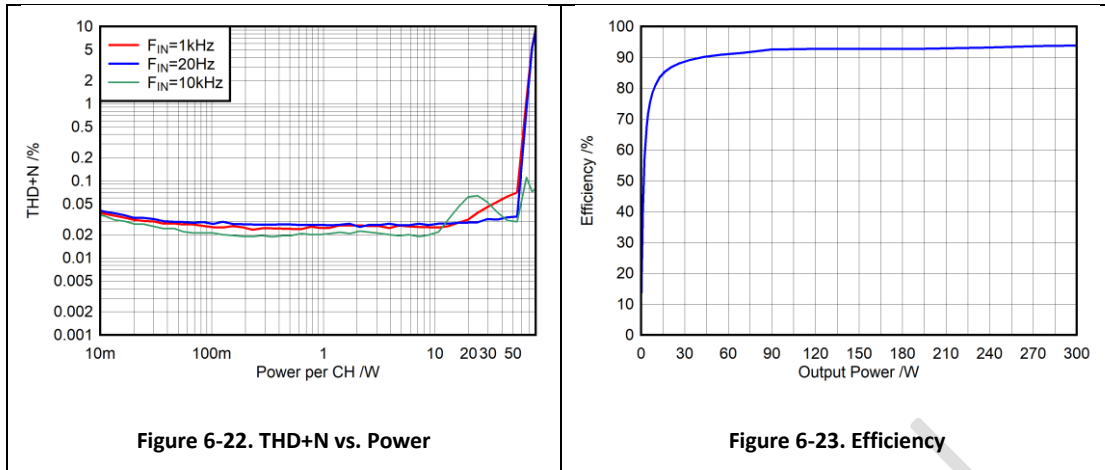
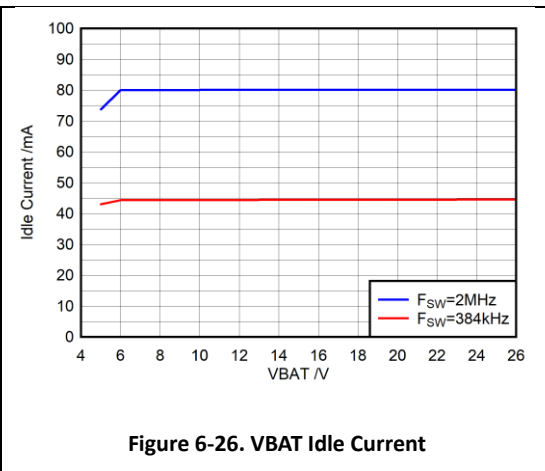
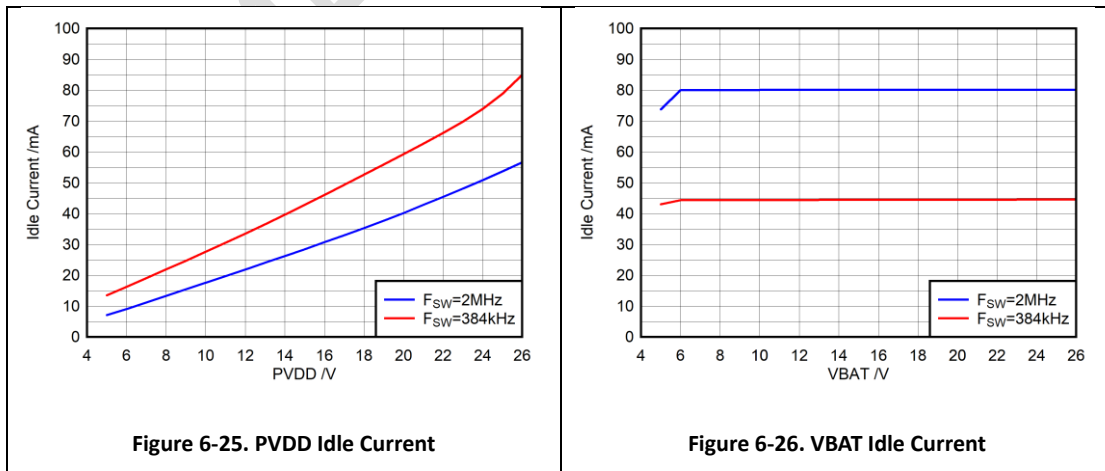


Figure 6-21. THD+N vs. Frequency



6.8.3 Idle Current and Noise

Test Condition: Ambient temperature = 25°C, PVDD = VBAT = 14.4V, VDD = 3.3V, $R_L = 4\Omega$, $P_{OUT} = 1W/ch$, $f_{IN} = 1kHz$, $F_{SW} = 2MHz$, AES17 FILTER. LC filter = $3.3\mu H + 1\mu F$ for 2MHz F_{SW} and $10\mu H + 1\mu F$ for 384kHz, unless otherwise noted.



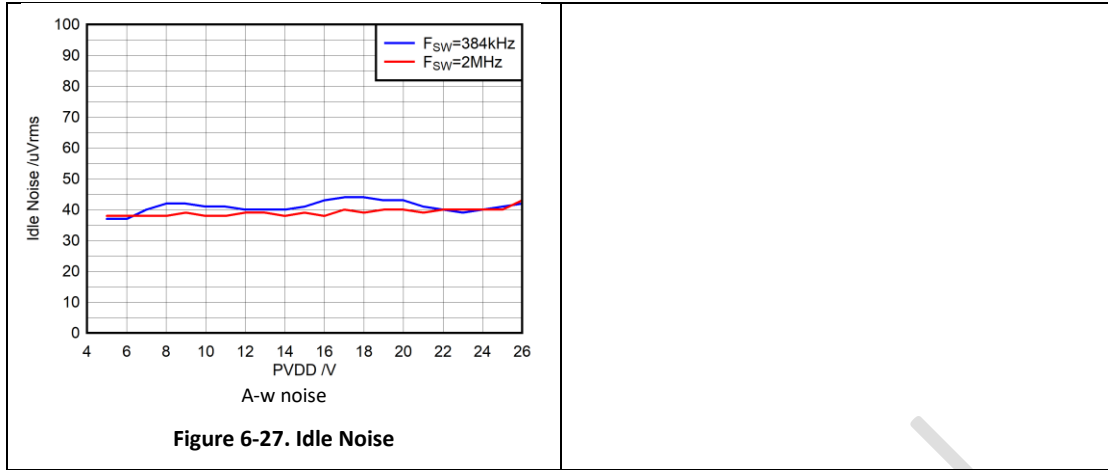


Figure 6-27. Idle Noise

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7. Detailed Descriptions

7.1 Overview

The ACM9634-Q1 is a 75W×4-channel digital input Class-D audio amplifier for the automotive industry. The device is designed for vehicle battery and boosted voltage operation. The device employs efficient Class-D technology that allows for high output power density and reduced power consumption and heat. The 2MHz operating frequency and low distortion modulation technology allows cost-effective inductors and minimized the solution size. The device integrates advanced EMC optimization features to address the possible issues in the system.

7.2 Serial Audio Port and Clocking

7.2.1 Clocks and Sample Rates

The serial audio interface port is a 3-wire serial port with the signals FSYNC/LRCLK, BCLK, and SDIN. BCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the ACM9634-Q1 device on the rising edge of BCLK. The FSYNC/LRCLK pin is the serial audio left/right word clock or frame sync when the device is operated in TDM mode. The SDIN consists two wires, SDIN1 and SDIN2. In TDM mode, SDIN1 is the data input. In I²S mode, SDIN1 is the data input for channel 1/2, and SDIN2 is the data input for channel 3/4.

The ACM9634-Q1 device has an audio sampling rate detection circuit that automatically detects the sampling frequency. Common audio sampling frequencies of 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz, 176.4kHz-192kHz are supported, as shown in **Table 7-1**. The sampling frequency detector sets the clock for DAC and audio effect tuning automatically.

The device has an internal PLL that is used to take the BCLK as reference clock and generate the higher rate clocks required by internal digital blocks.

Table 7-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	BCLK RATE (F _s)
I2S/LJ/RJ	32,24,20,16	32 to 96	64,32
TDM	32,24,20,16	32	128
		44.1/48	128,256,512
		96	128,256

7.2.2 Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I²S, left-justified, right-justified, and TDM/DSP data format. Data formats are selected via **DIG_I2S_DATA_FORMAT1**. If the high width of FSYNC/LRCLK in TDM/DSP mode is less than 8 cycles of BCLK, the bit [5:4] in **DIG_I2S_DATA_FORMAT1** should be set to 01. All formats require binary two's complement, MSB-first audio data, up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in **Table 7-2**. The data formats are detailed in **Figure 7-1** to **Figure 7-4**. The word length is selected in the bit [1:0] of **DIG_I2S_DATA_FORMAT1**. The offset of each channel is selected in **DIG_I2S_DATA_FORMAT2** to **DIG_I2S_DATA_FORMAT5**.

The TDM mode supports 4, 8 or 16 channels of audio data. The device can be configured through I²C to use different stereo pairs in the TDM data stream. The TDM mode supports 16-bit, 24-bit, and 32-bit input data lengths. In TDM mode, BCLK must be 128 x fs, 256 x fs or 512xfs, depending on the TDM slot size. **Table 7-2** lists register settings for the TDM channel selection.

Table 7-2. TDM Mode Audio Channel Selection

TDM Register DIG_I2S_DATA_FORMAT	CH1	CH2	CH3	CH4
0x00, 0x00, 0x00, 0x00	SLOT0	SLOT1	SLOT2	SLOT3

0x20, 0x20, 0x20, 0x20	SLOT1	SLOT2	SLOT3	SLOT4
0x80, 0x80, 0x80, 0x80	SLOT4	SLOT5	SLOT6	SLOT7
0x20, 0x40, 0x60, 0x80	SLOT1	SLOT3	SLOT5	SLOT7

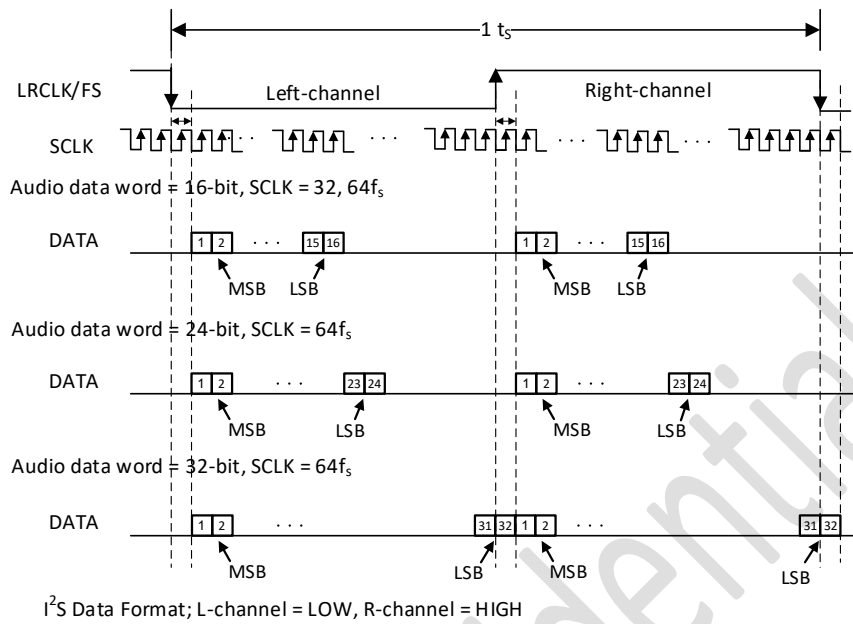


Figure 7-1. I²S Audio Data Format

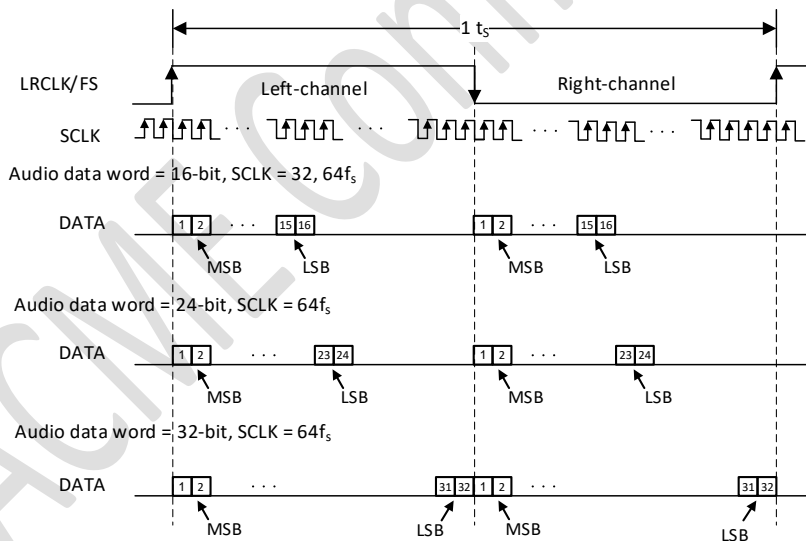


Figure 7-2. Left-Justified Audio Data Format

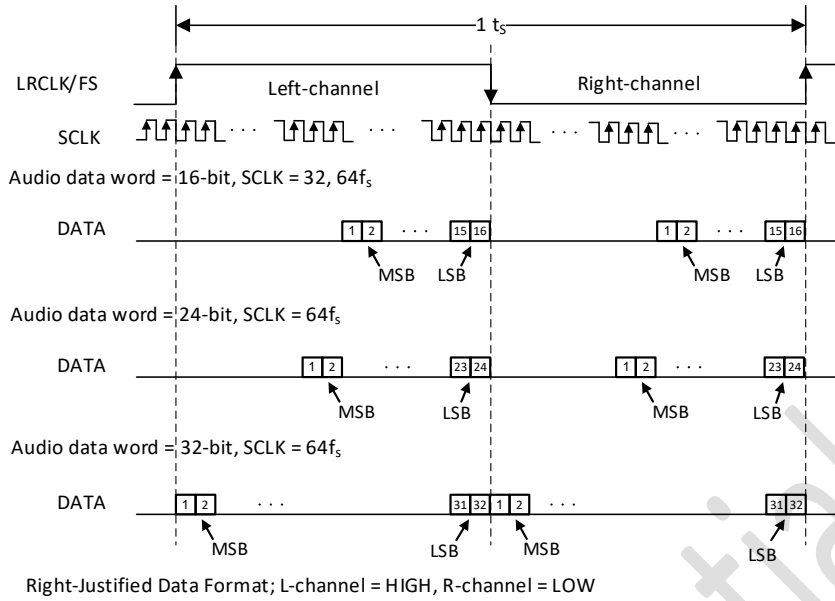


Figure 7-3. Right-Justified Audio Data Format

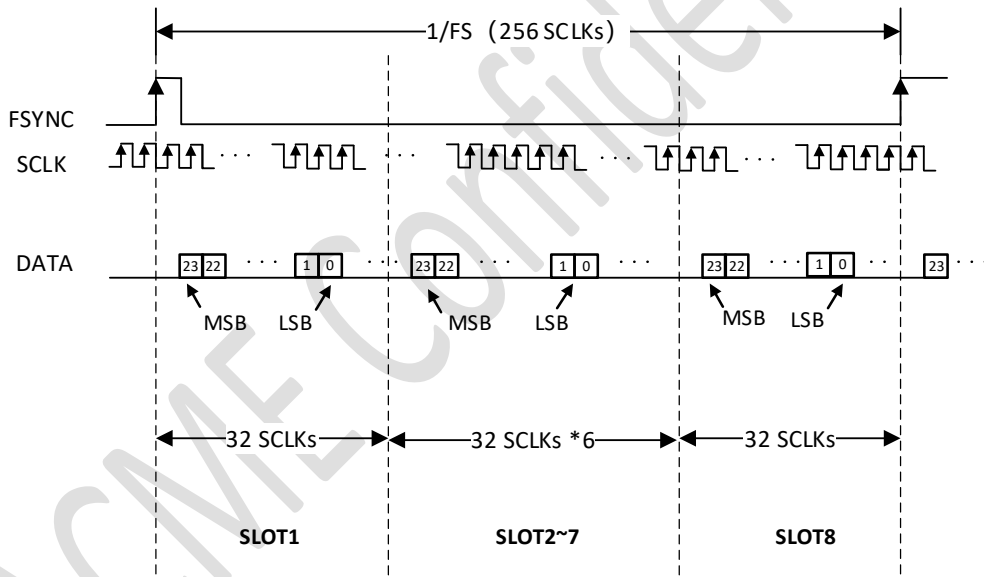


Figure 7-4. TDM8 Audio Data Format

8.3 DC Blocking

To remove the DC component on the output and protect the speakers, the ACM9634-Q1 integrates a high-pass filter on the audio signal path. The default cut-off frequency is 3-Hz, and is configurable in DSP.

8.4 Volume Control and Gain Structure

The analog gain, which is the peak output voltage swing at 0dBFS input, is configurable via I²C. The analog gain is independent among 4 channels. Table 7-3 lists the detail analog gain register settings.

Table 7-3. Analog Gain Register Settings - Channel 1 as Example

Register Value	Analog Gain	Analog Gain
----------------	-------------	-------------

<i>AMP_CTRL2</i>		dBV/FS
5'b00000	29.5 V/FS	26 dBV _{RMS} /FS
5'b00001	27.85 V/FS	25.5 dBV _{RMS} /FS
5'b00002	26.35 V/FS	25 dBV _{RMS} /FS
...
5'b11111	4.95 V/FS	10.5 dBV _{RMS} /FS

Besides, each channel has independent digital volume control. The range is from -110dB to 24dB and each step is 0.5dB.

8.5 High-Frequency Pulse-Width Modulating (PWM)

The PWM converts the digital input data into a switched signal of varying duty cycle. The high performance PWM modulator on ACM9634-Q1 has features as low noise, low distortion, and good stability. The ACM9634-Q1 has several switching frequencies options, as shown in Table 7-4. The option to switch at high frequency allows the use of smaller size and lower cost inductors.

Table 7-4. Switching Frequency Options

Register Value Page 0, Reg 0x01, bit [4:2]	Switching Frequency /kHz
3'b000	384
3'b010	480
3'b011	576
3'b100	768
3'b101	1536
3'b110	2048
3'b111	2340

8.6 Gate Driver and Power MOSFETs

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high current, H-bridge stage formed by power MOSFETs. The gate driver is powered by GVDD, which is generated by internal LDO. The decoupling capacitor for GVDD must be placed as close as possible to the pin 33 and pin 34.

The power stage of each channel is formed by 4 N-MOSFETs as an H-bridge. Therefore, bootstrap capacitors are required for the normal operation of the high side N-MOSFETs. A 0.47μF ceramic capacitor with 16V and X7R rated or better, is recommended. The bootstrap capacitors should be connected between the OUTx pin and the corresponding BSTx pin, as shown in **Figure 11-1**. The bootstrap capacitors function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high to maintain the high side MOSFETs turned on.

The ACM9634-Q1 employs low $R_{ds(on)}$ N-MOSFETs, which is typically 60mΩ, to achieve high efficiency, good thermal and maximize the output power from a given power supply voltage rail. These N-MOSFETs are designed to run in high switching frequency and could stand withstand large voltage transients during load dump event.

8.7 Load Diagnostics

The ACM9634-Q1 supports DC load diagnostic, AC load diagnostic and real-time load diagnostic to check the load status. The DC load diagnostic is run out of the Play mode and is capable to report short-to-power(S2P), short-to-ground(S2G), short-load(SL) or open-load(OL) fault. The AC load diagnostic is also run out of the Play mode, and is capable to report the impedance and phase of the load. The real-time load diagnostic monitors the load status during the music playing and is capable to report the open load and short load fault, without introducing any audio artifact.

The ACM9634-Q1 reports the detected fault via I²C bus or GPIOs and allows the flexibility of load fault handling by register configurations.

8.7.1 DC Load Diagnostic

The DC load diagnostics are used to verify the load connections. The DC load diagnostic could be triggered in two ways. The first way is the automatically execution when the device leaves the Deep Sleep mode or Sleep state, and enters either state of HiZ/Play/Mute. If a fast start-up is preferred, the DC load diagnostic could be bypassed by register setting. The second way to trigger the DC load diagnostic is manually setting any one or any count of the output channels to DC Load diagnostic state. The DC Load diagnostics doesn't rely on any external clock source, thus the manually trigger could be initiated at any time and in any device state as long as the power supplies are ready and the device is enabled by pulling the PDN to high.

The ACM9634-Q1 integrates unique circuits on the power stage for stimulus generation and signal acquisition to accomplish the DC load diagnostic. The ACM9634-Q1 supports various I²C configurable detail optimizing settings to make sure the DC load diagnostic procedure is fast and quiet. The DC load diagnostic covers four type of load faults, including short-to-power(S2P), short-to-ground(S2G), short-load (SL) or open-load (OL). In addition, ACM9634-Q1 supports the load diagnostic in line-out mode. In a full DC load diagnostic cycle, the S2P and S2G are executed firstly followed by the SL and OL detection. Each detection could be bypassed by register setting. The DC load diagnostics are run in parallel among the 4 channels to minimize the time consumption. Once a load fault detected, the same detection is automatically repeated to confirm the fault condition before moving to next load fault detection.

In S2P and S2G detections, the device detects whether there is short condition to power lines by measuring the dc resistance between each output pin and PVDD/GND pin. The ACM9634-Q1 supports adjustable S2P and S2G threshold, which makes it capable to detect the soft short or the short to battery in the boosted PVDD systems. **Figure 7-5** and **Figure 7-6** shows the S2P and S2G reporting thresholds.

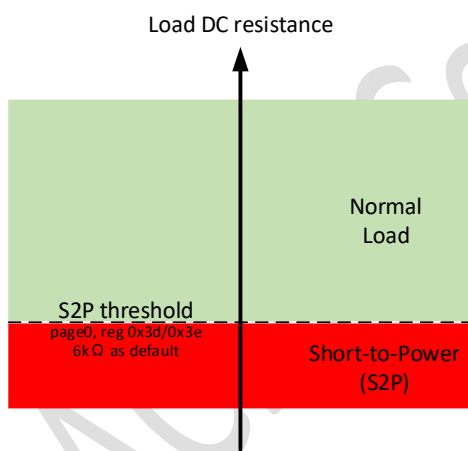


Figure 7-5. S2P Reporting Thresholds

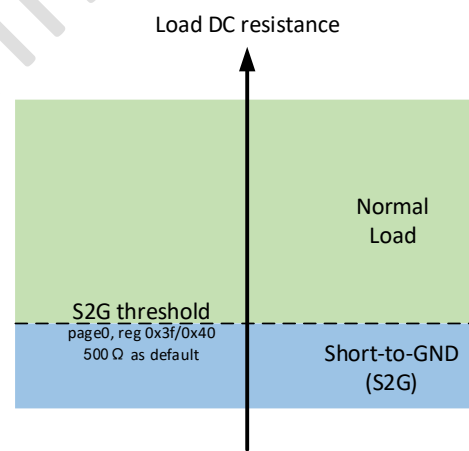


Figure 7-6. S2G Reporting Thresholds

In SL and OL detections, the device measures the dc resistance between OUTxP and OUTxN to determine whether there is short or open load condition, as shown in **Figure 7-7**. The ACM9634-Q1 supports channel independent SL threshold setting in registers from **DIG_DC_DIAG_SL_DET_THRESHOLD**. The OL threshold is configured by **DIG_DC_DIAG_OL_DET_THRESHOLD**.

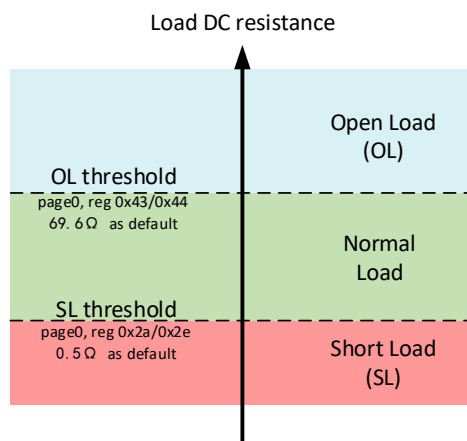


Figure 7-7. SL/OL Reporting Thresholds - Channel 1 as Example

8.7.2 DC Load diagnostics in Line-out Mode

In line-out applications, the OL threshold is configured by *DIG_DC_DIAG_LINEOUT_DET_THRESHOLD*, as shown in Figure 7-8. The load resistance measurement results are available in registers *DIG_DC_DIAG_RPT*.

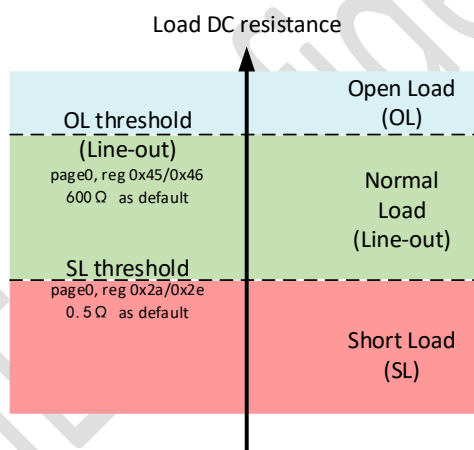


Figure 7-8. SL/OL Reporting Thresholds in Line-out Mode – Channel 1 as Example

For more detail descriptions, please refer to *ACM9634-Q1 Technical Reference Manual*.

8.7.3 AC Load Diagnostic

The ACM9634-Q1 supports AC load diagnostic, which measures the load complex impedance and phase at specific frequency to check the load status. AC load diagnostic is a good complement to DC load diagnostic especially for the circumstance where there is an AC coupled speaker. The ACM9634-Q1 does not rely on any external stimulus signal to run the AC load diagnostic. The ACM9634-Q1 is capable to generate various stimulus in wide frequency range, which is configured in register *DIG_DC_DIAG_AC_FREQ* and *DIG_NCO_MAX*. The AC load diagnostic is controlled via I²C and could be start in any device state. The AC load diagnostic could be independently run on one specific channel, or simultaneously run on multiple channels, which minimizes the diagnostic time consumption. Figure 7-9 shows the recommended sequence to run an AC load diagnostic.

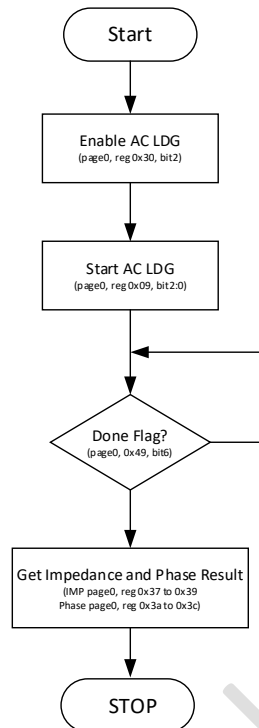


Figure 7-9. AC Load Diagnostic - Channel 1 as Example

For more detail descriptions, please refer to *ACM9634-Q1 Technical Reference Manual*.

8.7.4 Real-time Load Diagnostic

In Play state, the ACM9634-Q1 continuously monitors the real-time output voltage and the current flowing into the load and is capable to report the open-load and short-load fault, as known as the real-time load diagnostic. For the real-time open-load detection, the criterion is a low load current observed when the output voltage is high, and the situation lasts longer than the user defined time window. **Figure 7-10** illustrates the concept of real-time open-load diagnostic with a piece of music snapshot. For the real-time short-load detection, the criterion is a high load current observed when the output voltage is low, and the situation lasts longer than the user defined time window. The “high” and “low” are determined by comparing with register configurable thresholds. **Figure 7-11** illustrates the concept of real-time short-load diagnostic with a piece of music snapshot.

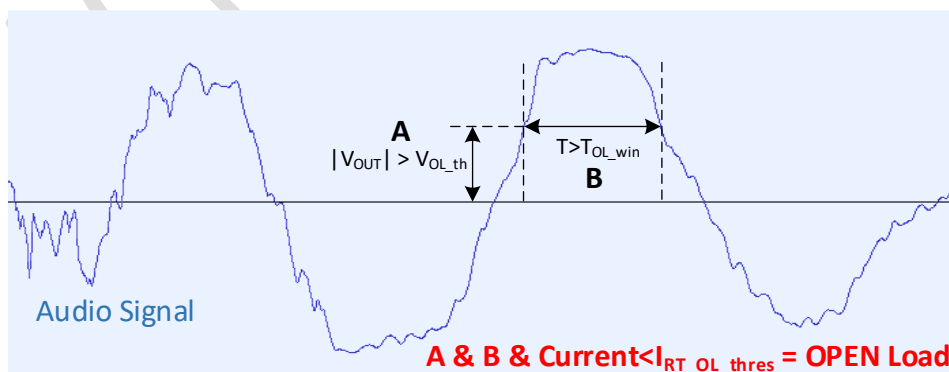


Figure 7-10. Concept of Real-time Open-load Diagnostic

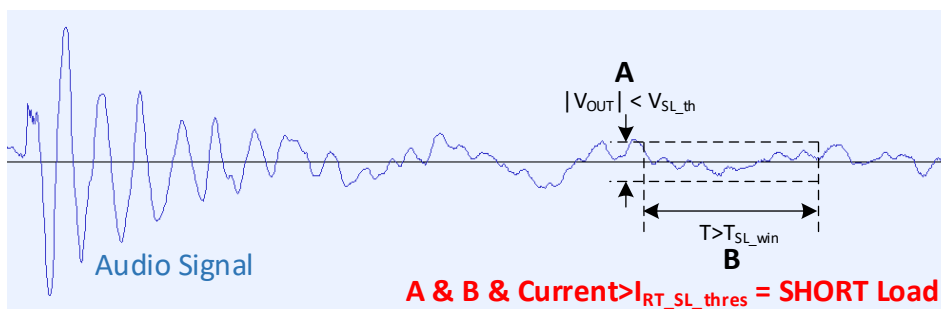


Figure 7-11. Concept Of Real-time Short-load Diagnostic

The real-time load diagnostic is enabled or disabled in register *DIG_DSP_CTRL*. The real-time load diagnostic fault flags locate in register *DIG_FAULT_RPT5*. Once a real-time load diagnostic fault flag is set, the related channel could either stop playing the music and transfer to the Sleep state, or keep playing the music, which is controlled in register *DIG_MISC_CTRL*.

For more detail descriptions, please refer to *ACM9634-Q1 Technical Reference Manual*.

8.8 Low EMI Considerations

The good EMC performance relies on both sophisticated integrated circuit design and careful system level design. The ACM9634-Q1 has several features to minimize the EMI from the integrated circuit, including inter-channel/chip phase shift, slew rate control and spread-spectrum.

8.8.1 Inter-channel Phase Shift

The ACM9634-Q1 supports two inter-channel phase shift schemes, which are 0/180/90/270 degree and 0/90/180/270 degree. The inter-channel phase shift is configured in register *DIG_SS_CTRL1*. The phase shift helps to decrease the ripple on the PVDD supply rail and reduce the both the conducted and emitted EMI.

8.8.2 Inter-chip Phase Shift

The ACM9634-Q1 supports phase synchronization among multiple devices, which helps to minimize the ripple on power lines and improve EMC performance. The PWM phase of each device could be synchronized to the audio serial input clock, or an external clock input from a user defined GPIO, as shown in Figure 7-12 and Figure 7-13. There are four options as 0/45/90/135 degree in total. The synchronization setting locates on *DIG_SS_CTRL1*. In GPIO synchronization mode, the device would not start to switch until a negative edge is observed on the GPIO pin.

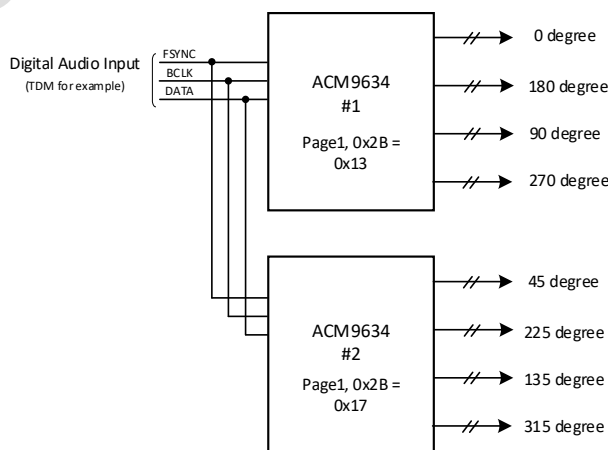


Figure 7-12. Multiple Device Switching Phase Synchronization by Digital Audio Input

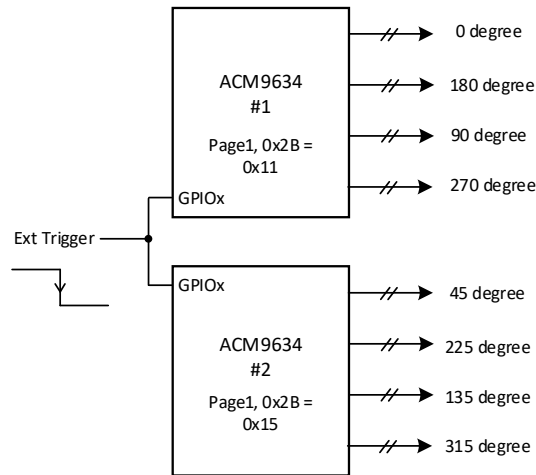


Figure 7-13. Multiple Device Switching Phase Synchronization by External GPIO

8.8.3 Slew Rate Control

The ACM9634-Q1 offers user configurable slew rate in register **AMP_CTRL2**. A lower slew rate reduces the high frequency harmonic intensity on the PWM output. As the high frequency noise on switching node dominates the source of EMI, a slower slew rate could significantly decrease the conducted and emitted emission. On the other hand, a lower slew rate increases the switching loss and decrease the efficiency. Therefore, it is recommended to carefully achieve the balance between the EMC performance and efficiency.

8.8.4 Spread Spectrum

Spread Spectrum distributes the narrowband PWM switching signal into a wideband signal, which spreads the energy across a specific frequency range. The ACM9634-Q1 offers several spread spectrum options to improve the EMC performance, including the spread-spectrum range and modulation period. The spread spectrum settings locate in **DIG_SS_CTRL** registers.

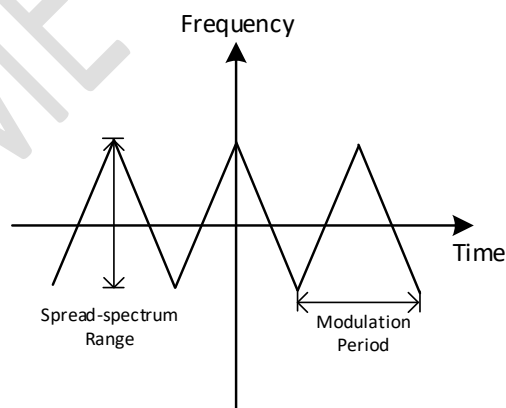


Figure 7-14 Triangle Spread Spectrum

For more detail spread spectrum descriptions, please refer to *ACM9634-Q1 Technical Reference Manual*.

8.9 Protections and Monitoring

8.9.1 Over Current Protection

If the output current exceeds the over current shutdown threshold, I_{SD} , such as the any of the output suddenly short to GND or power supply, an over current shutdown (OCSD) event is triggered. Each channel is monitored, limited, and reported independently. Once an OCSD is triggered, the device shuts down the affected channel and transfer its state to Sleep.

By default, the OCSD event is reported as fault to register and FAULT pin.

To recover from fault condition and back to normal operation, the user needs to write to bit 7 of the **AMP_CTRL1** to clear the fault. Then the device will start with a DC load diagnostic to check the load status. The device would not turn on the output stage and enter Play state until the load diagnostic is passed. This mechanism protects the output stage from repetitively high current rush.

8.9.2 DC Detection

The ACM9634-Q1 monitors the DC offset continuously during normal operation at the output. If any channel's DC output exceeds the DC_{DETECT} threshold, the channel triggers a DC Fault Event and is transferred to Sleep state.

By default, the DC event is reported as fault to register and FAULT pin.

8.9.3 Clip Detection

The ACM9634-Q1 monitors the output signal for voltage clipping situation. Each channel is monitored and reported independently. The clip level to create a clip event could be configured in the DSP registers.

By default, the Clip event is reported as warning to register and WARN pin.

8.9.4 Over-temperature Warning and Shutdown

The ACM9634-Q1 integrates five temperature sensors in total, as shown in **Figure 7-15**.

The global temperature sensor locates in the central position of the die. It is mostly used to monitor the junction temperature of the device. The channel temperature sensors locate on the output power FETs. They can be used to monitor the local temperature where the heat is mostly concentrated.

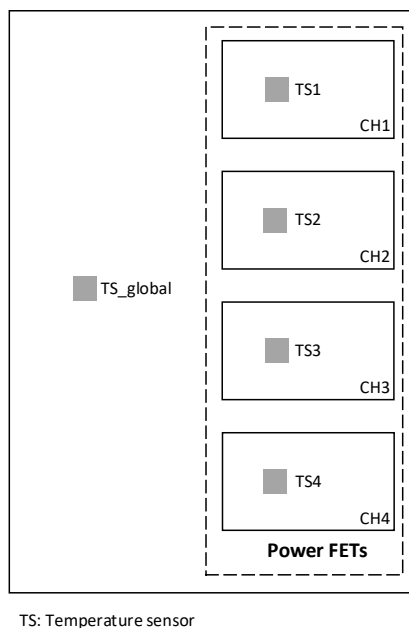


Figure 7-15. Temperature Sensors in the Device

8.9.4.1 Global Over-temperature Warning and Shutdown

The global temperature sensor monitors the die surface temperature and generates the global over-temperature warning (global OTW) and global over-temperature shutdown (global OTSD) based on the settings in *DIG_STATE_CTRL1*.

By default, the global OTW event is reported as warning to register and WARN pin, and the global OTSD is reported as fault to register and FAULT pin.

8.9.4.2 Channel Over-temperature Warning and Shutdown

Each independent channel has 8 OTW threshold options, which is configured in *DIG_STATE_CTRL2* to *DIG_STATE_CTRL5*. The channel OTSD threshold setting locates in *ANA_CTRL2*. It is shared among 4 channels.

By default, the global OTW event is reported as warning to register and WARN pin, and the global OTSD is reported as fault to register and FAULT pin.

8.9.5 PVDD and Temperature Sense

The ACM9634-Q1 integrates SAR ADCs to sense and report the real-time PVDD supply voltage and die temperature. The conversions are active in HiZ and Play state. The PVDD result is available in *DIG_PTSNS_RPT1*, with 0.156V/code.

The die temperature result is available in *DIG_PTSNS_RPT2*, with the conversion equation as below,

$$\text{Die Temperature}(\text{°C}) = -57 + \text{code in DEC}$$

It should be noted that the die temperature is acquired from the global temperature sensor, which could be lower than the channel temperature.

By default, the PVDD and temperature conversions are both enabled. These functions could be disabled in *DIG_PTSNS_CTRL*.

8.9.6 Over voltage and Load-dump

When PVDD supply voltage rises above the V_{PVDD_OV} , or the VBAT supply voltage rises above the V_{VBAT_OV} , the over voltage protection is triggered and the device enters Sleep state. When the PVDD supply voltage falls to the voltage lower than (V_{PVDD_OV}

- $V_{PVDD_OV_HYS}$) and VBAT supply voltage falls to voltage lower than $(V_{VBAT_OV} - V_{VBAT_OV_HYS})$, the device recovers normal operation automatically. The register fault flag and the pulled-low fault pin would not recover until the fault is cleared manually by writing to bit 7 of the **AMP_CTRL1**.

By default, the over voltage event is reported as fault to register and FAULT pin.

To meet the requirements of ISO7637, the device can withstand 40 V load dump voltage surges.

8.9.7 Undervoltage and Power-on-reset

When PVDD supply voltage falls below the V_{PVDD_UV} , or the VBAT supply voltage falls below the V_{VBAT_UV} , the undervoltage protection is triggered and the device enters Sleep state. When the PVDD supply voltage rises to the voltage higher than $(V_{PVDD_UV} + V_{PVDD_UV_HYS})$ and VBAT supply voltage falls to voltage lower than $(V_{VBAT_OV} + V_{VBAT_UV_HYS})$, the device recovers normal operation automatically. The register fault flag and the pulled-low fault pin would not recover until the fault is cleared manually by writing to bit 7 of the **AMP_CTRL1**.

By default, the undervoltage event is reported as fault to register and FAULT pin.

8.9.8 Clock Fault

The ACM9634-Q1 monitors the audio serial interface for clock fault detection. Once a clock fault event is triggered, the device enters HiZ state. The device recovers normal operation automatically when the fault condition is removed. The register fault flag and the pulled-low fault pin would not recover until the fault is cleared manually by writing to bit 7 of the **AMP_CTRL1**.

By default, the clock fault event is reported as fault to register and FAULT pin.

8.10 Power Supply Rails

The ACM9634-Q1 has three power supply inputs: DVDD, PVDD and VBAT. DVDD is a 3.3V or 1.8V supply rail that provides power to the digital domain. PVDD is the power supply rail that provides power for the output stage. VBAT is the power supply rail that provides the power for the whole analog domain except the power stage. Several on-chip regulators are included generating the voltages necessary for the internal circuitry. The external pins are provided only for bypass capacitors to filter the supply and should not be used to power other circuits.

8.10.1 Power-up Sequence

The ACM9634-Q1 could accept any sequence among DVDD, VBAT and PVDD. The PDN pin should be pulled up after the DVDD, VBAT and PVDD are ready. It is recommended to wait 5ms at least for the internal circuits power up before initializing the device via I²C bus.

The power up sequence is shown in **Figure 7-16**.

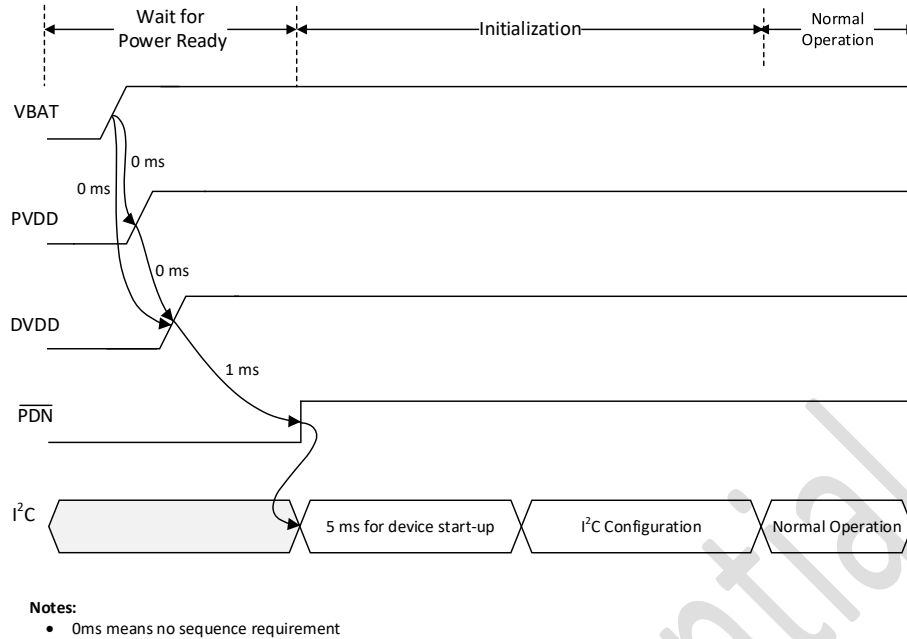
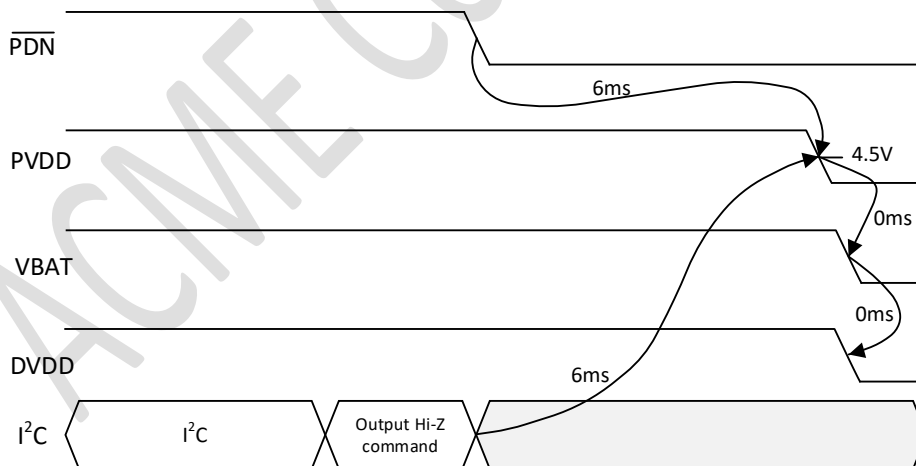


Figure 7-16. Power-up Sequence

8.10.2 Power-down Sequence

For the power down sequence, it is recommended to pull down the PDN first, wait at least 6ms for the volume ramp down and the power stage turned off. Finally, the DVDD, VBAT and PVDD can be removed without sequence requirement, as shown in Figure 7-17.



- Notes:**
- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{\text{PDN}}$ or by I2C command.
 - At least 6ms delay needed based on LRCLK (F_s) = 48kHz, Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume = 24dB.

Figure 7-17. Power-down Sequence

8.11 Hardware Control

The ACM9634-Q1 has several hardware control pins, such as the PDN pin and the GPIOs. Each GPIO could be configured as several functions, including MUTE, FAULT, WARN, SDOUT1/2, etc.

8.11.1 PDN

This pin is to power up and shutdown the device. When pulled high, the device is powered up, and vice versa.

8.11.2 MUTE

This active-high input pin is used for hardware control of the mute and unmute function for all channels.

8.11.3 FAULT

This pin reports faults and is active-low under any of the following conditions:

- Any channel faults (overcurrent or DC detection)
- Global over-temperature shutdown
- Overvoltage or undervoltage conditions on the VBAT or PVDD pins
- Clock errors
- Real-time load faults
- Cycle-by-cycle current limit faults

Specific fault categories could be masked by related register bits from reporting to the FAULT pin. These bits only mask the setting of the pin and do not affect the register reporting or protection of the device. By default, all faults are reported to the pin.

When configured as Fault, the GPIO pin is an open-drain output and require a pull-up resistor to DVDD.

The FAULT pin is latched and can be cleared by writing the **CLEAR FAULT** bit in register **AMP_CTRL1**.

8.11.4 WARN

This pin reports faults and is active-low under any of the following conditions:

- Channel over-temperature warning
- Clipping
- Global over-temperature warning
- Cycle-by-cycle current limit warning

Specific warning categories could be masked by related register bits from reporting to the WARN pin. These bits only mask the setting of the pin and do not affect the register reporting. By default, all the warnings are reported to the pin.

When configured as WARN, the GPIO pin is an open-drain output and require a pull-up resistor to DVDD.

The WARN pin is not latched and is automatically cleared after the warning conditions removed.

8.12 Class-H Operation

The ACM9634-Q1 integrates Class-H Control feature, which provides a new scheme to increase efficiency and reduce power dissipation for battery powered system. The ACM9634-Q1 internal Class-H block monitors the digital audio signal, feeds the control signal to feedback network of the external boost convertor and adjusts boost convertor's V_{OUT} accordingly. Therefore, the power supply voltage rail dynamically tracks with the audio output signal and the best system efficiency and lowest power dissipation is achieved, as shown in **Figure 7-18**.

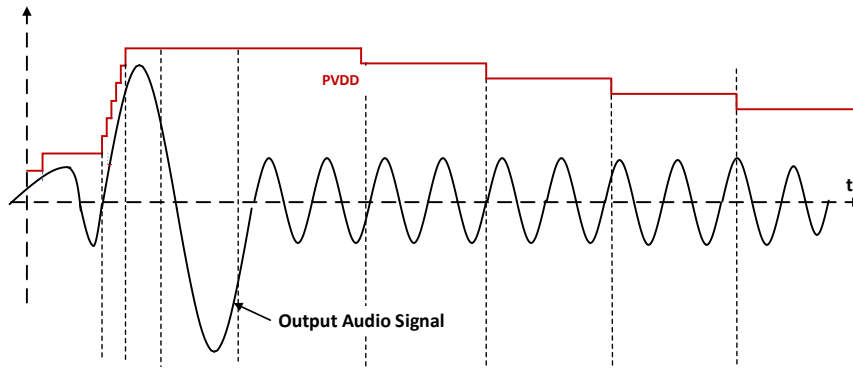


Figure 7-18. Class-H Operation

ACM9634-Q1 employs an internal Audio Signal Amplitude Detection Block for audio signal amplitude detection, as the target PVDD range and the amplifier system gain is known, so the digital input levels in 'Levels to PWM' block will calculate the proper digital input levels and transfers to different duty cycle. Generally, the ACM9634-Q1 supports 16 levels Class H Control. For example, if the PVDD range is 14.4V-24V, the PVDD tracking with output audio signals by following values: { 14.40V, 15.04V, 15.68V, 16.32V, 16.96V, 17.60V, 18.24V, 18.88V, 19.52V, 20.16V, 20.80V, 21.44V, 22.08V, 22.72V, 24V}. Based on detailed system application requirement (PVDD min/max value, V_{FB} of the boost convertor, DVDD value, R2), ACME Audio Tuning software generates corresponding register configuration and external BOM which shown in Figure 7-19.

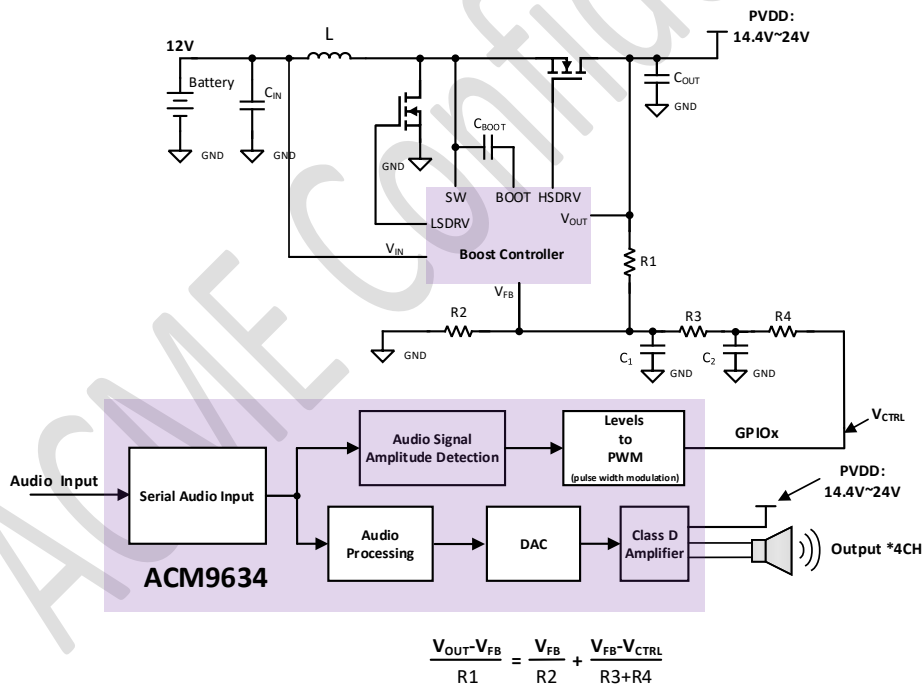


Figure 7-19. Simplified Class-H Application Circuit

8.13 Device Functional Modes

The ACM9634-Q1 operating modes are listed in Table 7-5.

Table 7-5. Device Functional Modes

STATE	DVDD Domain	Analog Domain	OUTPUT STAGE	I ² C
Shutdown	OFF	OFF	OFF	In-active
Deep Sleep	ON	OFF	OFF	Active
Sleep	ON	OFF	OFF	Active
HiZ	ON	ON	OFF	Active
Play	ON	ON	ON	Active

9. Programming

9.1 I²C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a slave device.

9.2 Slave Address

The ACM9634-Q1 device has 7 bits for the slave address. The first four bits (MSBs) of the slave address are factory preset to 0101 (0x5x). The next three bits of address byte are the device select bits which can be user-defined by ADR pin in Table below.

ADR Pin Configuration	MSBs				User Define			LSB	Device Write Address
4.7kΩ to DVDD	0	1	0	1	0	0	0	R/W	0x50
15kΩ to DVDD	0	1	0	1	0	0	1	R/W	0x52
47kΩ to DVDD	0	1	0	1	0	1	0	R/W	0x54
17kΩ to GND	0	1	0	1	0	1	1	R/W	0x56
47kΩ to GND	0	1	0	1	1	0	0	R/W	0x58
150kΩ to GND	0	1	0	1	1	0	1	R/W	0x5a

9.3 Random Write

As shown in Figure below, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

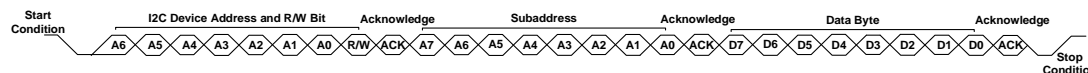


Figure 8-1. Random Write Transfer

9.4 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in Figure below. After receiving each data byte, the device responds with an acknowledge bit

and the I²C sub-address is automatically incremented by one.

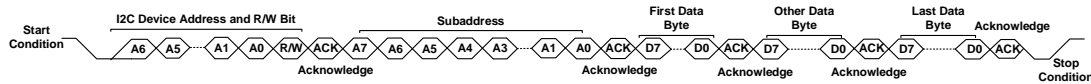


Figure 8-2. Sequential Write

9.5 Random Read

As shown in Figure below, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

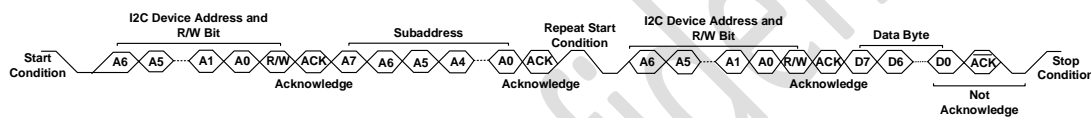


Figure 8-3. Random Read

9.6 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in Figure below. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

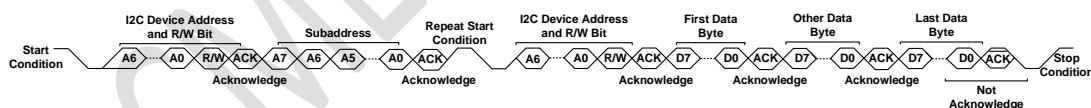


Figure 8-4. Random Read

8.7 Checksum

This device supports two different checksum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums, and both are available together simultaneously. The checksums can be reset by writing a starting value (e.g. 0x 00 00 00 00) to their respective 4-byte register locations.

8.8 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x07 polynomial (CRC-8-CCITT I.432.1, ATM HEC, ISDN HEC and cell delineation, $1 + x^1 + x^2 + x^8$). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I²C transactions, excluding the page switching. The CRC checksum is read from **DIG_CRC_CHECKSUM**.

The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

8.9 XOR Checksum

The XOR checksum is a simple checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR checksum is read from **DIG_XOR_CHECKSUM**. The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

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9. Register Map

9.1 Register Summary

Table 8-1. Register Table (Page 0)

Address	Type	Register Name	Default Value	Function Description
0x01	R/W	AMP_CTRL1 (Page 0, Offset=1h) [Reset=0x00]	0x00	Fault clear, BTL/PBTL selection, Switching frequency setting, Modulation mode
0x02	R/W	AMP_CTRL2 (Page 0, Offset=2h) [Reset=0x00]	0x00	Slew Rate Control, CH1 analog gain setting
0x03	R/W	AMP_CTRL3	0x00	CH2 analog gain setting
0x04	R/W	AMP_CTRL4	0x00	CH3 analog gain setting
0x05	R/W	AMP_CTRL5	0x00	CH4 analog gain setting
0x06	R/W	ANA_CTRL1	0x00	Bandwidth setting, power save setting
0x08	R/W	DIG_STATE_CTRL1	0x00	Reset Register, reset signal path, Reset DSP, Global OTW threshold
0x09	R/W	DIG_STATE_CTRL2	0x00	CH1 OTW threshold, CH1 Mute, CH1 states control
0x0a	R/W	DIG_STATE_CTRL3	0x00	CH2 OTW threshold, CH2 Mute, CH2 states control
0x0b	R/W	DIG_STATE_CTRL4	0x00	CH3 OTW threshold, CH3 Mute, CH3 states control
0x0c	R/W	DIG_STATE_CTRL5	0x00	CH4 OTW threshold, CH4 Mute, CH4 states control
0x0d	R/W	DIG_DSP_CTRL	0x6d	Real-time SL enable/disable, Real-time OL enable/disable, EQ control
0x10	R/W	DIG_I2S_DATA_FORMAT1	0x02	Audio data input format
0x11	R/W	DIG_I2S_DATA_FORMAT2	0x00	I2S/TDM data shift bits for CH1, bit [7:0]
0x12	R/W	DIG_I2S_DATA_FORMAT3	0x00	I2S/TDM data shift bits for CH2, bit [7:0]
0x13	R/W	DIG_I2S_DATA_FORMAT4	0x00	I2S/TDM data shift bits for CH3, bit [7:0]
0x14	R/W	DIG_I2S_DATA_FORMAT5	0x00	I2S/TDM data shift bits for CH4, bit [7:0]
0x15	R/W	DIG_TARGET_VOL_CH1	0xCF	Volume setting for CH1
0x16	R/W	DIG_TARGET_VOL_CH2	0xCF	Volume setting for CH2
0x17	R/W	DIG_TARGET_VOL_CH3	0xCF	Volume setting for CH3
0x18	R/W	DIG_TARGET_VOL_CH4	0xCF	Volume setting for CH4
0x1a	R/W	DIG_I2S_BAK2	0x01	I2S/TDM data shift bits for CH1/2/3/4, MSB
0x1f	R/W	DIG_SS_CTRL	0x20	Spread spectrum control
0x23	R/W	DIG_RTLDG_OL_CTRL	0xdd	Real time load diagnostic control
0x25	R/W	DIG_MISC_CTRL	0x08	Digital Miscellaneous control
0x26	R/W	DIG_PTSNS_CTRL	0x03	OTSD auto-recovery, PVDD sense enable/disable, Temperature sense enable/disable
0x27	R/W	DIG_ANA_CTRL_BAK	0x00	CLIP detection mode selection
0x28	R/W	ANA_CTRL3	0x00	Real-time open load enable/disable(analog domain), GVDD voltage adjust, 7V UVLO selection
0x2a	R/W	DIG_DC_DIAG_SL_DET_TH RESHOLD1	0x36	DC load diagnostic, short load threshold for CH1, bit [7:0]
0x2b	R/W	DIG_DC_DIAG_SL_DET_TH RESHOLD2	0x36	DC load diagnostic, short load threshold for CH2, bit [7:0]
0x2c	R/W	DIG_DC_DIAG_SL_DET_TH RESHOLD3	0x36	DC load diagnostic, short load threshold for CH3, bit [7:0]
0x2d	R/W	DIG_DC_DIAG_SL_DET_TH RESHOLD4	0x36	DC load diagnostic, short load threshold for CH4, bit [7:0]
0x2e	R/W	DIG_DC_DIAG_SL_DET_TH RESHOLD5	0x00	DC load diagnostic, short load threshold for CH1/2/3/4, MSB
0x30	R/W	DIG_DC_DIAG_CTRL1	0x15	DC load diagnostic control
0x31	R/W	DIG_DC_DIAG_CTRL2	0x77	CH1/2 DC load diagnostic test item control
0x32	R/W	DIG_DC_DIAG_CTRL3	0x77	CH3/4 DC load diagnostic test item control
0x34	R/W	DIG_DC_DIAG_AC_FREQ1	0x99	AC load diagnostic stimulus frequency setting, bit [7:0]
0x35	R/W	DIG_DC_DIAG_AC_FREQ2	0x99	AC load diagnostic stimulus frequency setting, bit [15:8]
0x36	R/W	DIG_DC_DIAG_AC_FREQ3	0x01	AC load diagnostic stimulus frequency setting, bit [23:16]
0x3a	R/W	DIG_DC_DIAG_S2PS2G_STI	0xc8	DC load diagnostic S2G/S2P bias current setting
0x3b	R/W	DIG_DC_DIAG_SLOL_STI	0xdc	DC load diagnostic SL/OL bias current setting
0x3c	R/W	DIG_DC_DIAG_LINEOUT_S TI	0x32	DC load diagnostic line out mode bias current setting
0x3d	R/W	DIG_DC_DIAG_S2P_DET_T HRESHOLD1	0xc0	DC load diagnostic S2P threshold, bit [7:0]
0x3e	R/W	DIG_DC_DIAG_S2P_DET_T	0x03	DC load diagnostic S2P threshold, bit [13:8]

		HRESHOLD2		
0x3f	R/W	DIG_DC_DIAG_S2G_DET_T HRESHOLD1	0xc0	DC load diagnostic S2G threshold, bit [7:0]
0x40	R/W	DIG_DC_DIAG_S2G_DET_T HRESHOLD2	0x03	DC load diagnostic S2G threshold, bit [13:8]
0x41	R/W	DIG_DC_DIAG_SLOL_DET_ GAIN	0xff	DC load diagnostic SL/OL ADC gain setting
0x43	R/W	DIG_DC_DIAG_OL_DET_TH RESHOLD1	0x64	DC load diagnostic OL threshold, bit [7:0]
0x44	R/W	DIG_DC_DIAG_OL_DET_TH RESHOLD2	0x19	DC load diagnostic OL threshold, bit [13:8]
0x45	R/W	DIG_DC_DIAG_LINEOUT_D ET_THRESHOLD1	0x00	DC load diagnostic OL threshold in line out mode, bit [7:0]
0x46	R/W	DIG_DC_DIAG_LINEOUT_D ET_THRESHOLD2	0x0c	DC load diagnostic OL threshold in line out mode, bit [13:8]
0x47	R/W	DIG_DC_DET_FACTOR1	0x1b	DC load diagnostic, DAC settling time setting. SL/OL decimation filter setting.
0x48	R/W	DIG_DC_DET_FACTOR2	0x1b	DC load diagnostic, DAC settling time setting. Decimation filter setting in line out mode.
0x49	RO	DIG_DC_DIAG_RPT1	0x00	DC load diagnostic fault report, CH1
0x4a	RO	DIG_DC_DIAG_RPT2	0x00	DC load diagnostic fault report, CH2
0x4b	RO	DIG_DC_DIAG_RPT3	0x00	DC load diagnostic fault report, CH3
0x4c	RO	DIG_DC_DIAG_RPT4	0x00	DC load diagnostic fault report, CH4
0x4d	RO	DIG_DC_DIAG_RPT5	0x00	DC load diagnostic S2P, S2G pin report CH1/2
0x4e	RO	DIG_DC_DIAG_RPT6	0x00	DC load diagnostic S2P, S2G pin report CH3/4
0x4f	RO	DIG_DC_DIAG_RPT7	0x00	DC load diagnostic load DC resistance result, bit [7:0], CH1
0x50	RO	DIG_DC_DIAG_RPT8	0x00	DC load diagnostic load DC resistance result, bit [7:0], CH2
0x51	RO	DIG_DC_DIAG_RPT9	0x00	DC load diagnostic load DC resistance result, bit [7:0], CH3
0x52	RO	DIG_DC_DIAG_RPT10	0x00	DC load diagnostic load DC resistance result, bit [7:0], CH4
0x53	RO	DIG_DC_DIAG_RPT11	0x00	DC load diagnostic load DC resistance result, bit [13:8], CH1/2
0x54	RO	DIG_DC_DIAG_RPT12	0x00	DC load diagnostic load DC resistance result, bit [13:8], CH3/4
0x60	RO	DIG_STATE_RPT_CH12	0x00	Channel state report, CH1/2
0x61	RO	DIG_STATE_RPT_CH34	0x00	Channel state report, CH3/4
0x62	RO	DIG_FAULT_RPT1	0x00	Fault report, DC and OCSD
0x63	RO	DIG_FAULT_RPT2	0x00	Fault report, OTW and OTSD
0x64	RO	DIG_FAULT_RPT3	0x00	Fault report, CLIP, OTP load failure, clock fault
0x65	RO	DIG_FAULT_RPT4	0x00	Fault report, CBC warning and fault
0x66	RO	DIG_FAULT_RPT5	0x00	Fault report, real-time load diagnostic fault
0x67	RO	DIG_FAULT_RPT6	0x00	Fault report, GVDD/PVDD/VBAT UV, PVDD/VBAT OV
0x68	RO	DIG_I2S_CLK_FORMAT_RP T1	0x00	BCLK and FSYNC frequency detection result
0x69	RO	DIG_I2S_CLK_FORMAT_RP T2	0x00	BCLK/FSYNC ratio detection result
0x6a	RO	DIG_PTSNS_RPT1	0x00	PVDD sense result
0x6b	RO	DIG_PTSNS_RPT2	0x00	Temperature sense result
0x6f	RO	Die ID	0x00	Die ID
0x7e	RO	DIG_XOR_CHECKSUM	0x00	XOR checksum
0x7f	RO	DIG_CRC_CHECKSUM	0x00	CRC checksum

Table 8-2. Register Table (Page 1)

Address	Type	Register Name	Default Value	Description
0x0c	R/W	DIG_RTLDG_SLOL_CTRL1	0x34	Real-time load diagnostic, short load detection window length setting, skip cycles setting
0x0d	R/W	DIG_I2S_CLK_FORMAT_LEVEL1	0x00	I2S/TDM clock rate setting
0x0f	R/W	DIG_I2S_CTRL2_LEVEL1	0x00	I2S/TDM clock enable/disable, polarity setting
0x2b	R/W	DIG_SS_CTRL1_LEVEL1	0x10	PWM phase control, inter-chip PWM phase sync setting
0x2c	R/W	DIG_SS_CTRL1_LEVEL1	0x00	Spread spectrum setting
0x37	RO	DIG_AC_DIAG_FULL_RPT1	0x00	CH1 AC load diagnostic impedance report, bit [23:16]
0x38	RO	DIG_AC_DIAG_FULL_RPT2	0x00	CH1 AC load diagnostic impedance report, bit [15:8]
0x39	RO	DIG_AC_DIAG_FULL_RPT3	0x00	CH1 AC load diagnostic impedance report, bit [7:0]
0x3a	RO	DIG_AC_DIAG_FULL_RPT4	0x00	CH2 AC load diagnostic impedance report, bit [23:16]
0x3b	RO	DIG_AC_DIAG_FULL_RPT5	0x00	CH2 AC load diagnostic impedance report, bit [15:8]
0x3c	RO	DIG_AC_DIAG_FULL_RPT6	0x00	CH2 AC load diagnostic impedance report, bit [7:0]
0x3d	RO	DIG_AC_DIAG_FULL_RPT7	0x00	CH3 AC load diagnostic impedance report, bit [23:16]
0x3e	RO	DIG_AC_DIAG_FULL_RPT8	0x00	CH3 AC load diagnostic impedance report, bit [15:8]
0x3f	RO	DIG_AC_DIAG_FULL_RPT9	0x00	CH3 AC load diagnostic impedance report, bit [7:0]
0x40	RO	DIG_AC_DIAG_FULL_RPT10	0x00	CH4 AC load diagnostic impedance report, bit [23:16]
0x41	RO	DIG_AC_DIAG_FULL_RPT11	0x00	CH4 AC load diagnostic impedance report, bit [15:8]
0x42	RO	DIG_AC_DIAG_FULL_RPT12	0x00	CH4 AC load diagnostic impedance report, bit [7:0]
0x43	RO	DIG_AC_DIAG_FULL_RPT13	0x00	CH1 AC load diagnostic phase report, bit [23:16]
0x44	RO	DIG_AC_DIAG_FULL_RPT14	0x00	CH1 AC load diagnostic phase report, bit [15:8]
0x45	RO	DIG_AC_DIAG_FULL_RPT15	0x00	CH1 AC load diagnostic phase report, bit [7:0]
0x46	RO	DIG_AC_DIAG_FULL_RPT16	0x00	CH2 AC load diagnostic phase report, bit [23:16]
0x47	RO	DIG_AC_DIAG_FULL_RPT17	0x00	CH2 AC load diagnostic phase report, bit [15:8]
0x48	RO	DIG_AC_DIAG_FULL_RPT18	0x00	CH2 AC load diagnostic phase report, bit [7:0]
0x49	RO	DIG_AC_DIAG_FULL_RPT19	0x00	CH3 AC load diagnostic phase report, bit [23:16]
0x4a	RO	DIG_AC_DIAG_FULL_RPT20	0x00	CH3 AC load diagnostic phase report, bit [15:8]
0x4b	RO	DIG_AC_DIAG_FULL_RPT21	0x00	CH3 AC load diagnostic phase report, bit [7:0]
0x4c	RO	DIG_AC_DIAG_FULL_RPT22	0x00	CH4 AC load diagnostic phase report, bit [23:16]
0x4d	RO	DIG_AC_DIAG_FULL_RPT23	0x00	CH4 AC load diagnostic phase report, bit [15:8]
0x4e	RO	DIG_AC_DIAG_FULL_RPT24	0x00	CH4 AC load diagnostic phase report, bit [7:0]
0x50	R/W	DIG_SDOUT_PAD_CTRL	0x29	GPIO function selection, SDOUT
0x51	R/W	DIG_GPIO0_PAD_CTRL	0x28	GPIO function selection, GPIO0 (default: WARN)
0x52	R/W	DIG_GPIO1_PAD_CTRL	0x00	GPIO function selection, GPIO1 (default: OFF)
0x53	R/W	DIG_GPIO2_PAD_CTRL	0x00	GPIO function selection, GPIO2 (default: OFF)
0x54	R/W	DIG_GPIO3_PAD_CTRL	0x2b	GPIO function selection, GPIO3 (default: FAULT)
0x55	R/W	DIG_GPIO4_PAD_CTRL	0x05	GPIO function selection, GPIO4 (default: MUTE)
0x56	R/W	DIG_VBAT_OVUV_SEL1	0xff	Fault mask setting1, OV/UV
0x57	R/W	DIG_VBAT_OVUV_SEL2	0xff	Fault mask setting2, OV/UV
0x58	R/W	DIG_FAULT_SDOUT_SEL	0xff	Fault/Warning mask setting1, SDOUT

		1		
0x59	R/W	DIG_FAULT_SDOU SEL2	0xff	Fault/Warning mask setting2, SDOU
0x5a	R/W	DIG_FAULT_SDOU SEL3	0xff	Fault/Warning mask setting3, SDOU
0x5b	R/W	DIG_FAULT_SDOU SEL4	0xff	Fault/Warning mask setting4, SDOU
0x5c	R/W	DIG_FAULT_SDOU SEL5	0xff	Fault/Warning mask setting5, SDOU
0x5d	R/W	DIG_FAULT_GPI0 SEL1	0xff	Fault/Warning mask setting1, GPIO0
0x5e	R/W	DIG_FAULT_GPI0 SEL2	0xff	Fault/Warning mask setting2, GPIO0
0x5f	R/W	DIG_FAULT_GPI0 SEL3	0xff	Fault/Warning mask setting3, GPIO0
0x60	R/W	DIG_FAULT_GPI0 SEL4	0xff	Fault/Warning mask setting4, GPIO0
0x61	R/W	DIG_FAULT_GPI0 SEL5	0xff	Fault/Warning mask setting5, GPIO0
0x62	R/W	DIG_FAULT_GPI1 SEL1	0xff	Fault/Warning mask setting1, GPIO1
0x63	R/W	DIG_FAULT_GPI1 SEL2	0xff	Fault/Warning mask setting2, GPIO1
0x64	R/W	DIG_FAULT_GPI1 SEL3	0xff	Fault/Warning mask setting3, GPIO1
0x65	R/W	DIG_FAULT_GPI1 SEL4	0xff	Fault/Warning mask setting4, GPIO1
0x66	R/W	DIG_FAULT_GPI1 SEL5	0xff	Fault/Warning mask setting5, GPIO1
0x67	R/W	DIG_FAULT_GPI2 SEL1	0xff	Fault/Warning mask setting1, GPIO2
0x68	R/W	DIG_FAULT_GPI2 SEL2	0xff	Fault/Warning mask setting2, GPIO2
0x69	R/W	DIG_FAULT_GPI2 SEL3	0xff	Fault/Warning mask setting3, GPIO2
0x6a	R/W	DIG_FAULT_GPI2 SEL4	0xff	Fault/Warning mask setting4, GPIO2
0x6b	R/W	DIG_FAULT_GPI2 SEL5	0xff	Fault/Warning mask setting5, GPIO2
0x6c	R/W	DIG_FAULT_GPI3 SEL1	0xff	Fault/Warning mask setting1, GPIO3
0x6d	R/W	DIG_FAULT_GPI3 SEL2	0xff	Fault/Warning mask setting2, GPIO3
0x6e	R/W	DIG_FAULT_GPI3 SEL3	0xff	Fault/Warning mask setting3, GPIO3
0x6f	R/W	DIG_FAULT_GPI3 SEL4	0xff	Fault/Warning mask setting4, GPIO3
0x70	R/W	DIG_FAULT_GPI3 SEL5	0xff	Fault/Warning mask setting5, GPIO3
0x71	R/W	DIG_FAULT_GPI4 SEL1	0xff	Fault/Warning mask setting1, GPIO4
0x72	R/W	DIG_FAULT_GPI4 SEL2	0xff	Fault/Warning mask setting2, GPIO4
0x73	R/W	DIG_FAULT_GPI4 SEL3	0xff	Fault/Warning mask setting3, GPIO4
0x74	R/W	DIG_FAULT_GPI4 SEL4	0xff	Fault/Warning mask setting4, GPIO4
0x75	R/W	DIG_FAULT_GPI4 SEL5	0xff	Fault/Warning mask setting5, GPIO4
0x76	R/W	DIG_IO_OPENDRAIN EN	0x3f	GPIO open-drain setting for Class-H function
0x77	R/W	DIG_IO_GVDD_FAULT SEL	0x3f	GVDD UV fault mask setting
0x78	R/W	DIG_OTW_GLOBAL SEL	0x3f	OTW/OTSD fault mask setting
0x79	R/W	DIG_DC_DIAG_FAULT SEL	0x30	DC Load diagnostic fault mask setting
0x80	R/W	DIG_FAULT_LATCH SEL	0xf0	Fault/Warning Latch selection

9.2 Detail Register Description

9.2.1 Page 0 Registers

9.2.1.1 AMP_CTRL1 (Page 0, Offset=1h) [Reset=0x00]

7	6	5	4	3	2	1	0
analog_fault_clear	pbt134	pbt112	fsw_sel[2:0]			hb_mode	damp_mode
R/W							

Bit	Field	Type	Reset	Description
7	analog_fault_clear	R/W	0	Force clear all latched analog fault
6	pbt134	R/W	0	0: CH3/4 pbt1 mode disable 1: CH3/4 pbt1 mode enable
5	pbt112	R/W	0	0: CH1/2 pbt1 mode disable 1: CH3/4 pbt1 mode enable
4:2	fsw_sel[2:0]	R/W	000	PWM frequency selection: 000: 384 kHz 001:310 kHz 010:480 kHz 011:576 kHz 100:768 kHz 101:1536 kHz 110:2048 kHz 111:2304 kHz
1	hb_mode	R/W	0	Modulation mode selection: Only if damp_mode=1 and hb_mode=1, chip is in hb_mode
0	damp_mode	R/W	0	Modulation mode selection: 0: BD 1: SPW

9.2.1.2 AMP_CTRL2 (Page 0, Offset=2h) [Reset=0x00]

7	6	5	4	3	2	1	0
SR[2:0]			ana_gain_ch1[4:0]				
R/W			R/W				

Bit	Field	Type	Reset	Description
7:5	SR[2:0]	R/W	000	Output slew rate control: 000:2.05 V/ns 001:2.47 V/ns 010:2.89 V/ns 011:3.31 V/ns 100:0.41 V/ns 101:0.82 V/ns 110:1.23 V/ns 111:1.64 V/ns
4:0	ana_gain_ch1[4:0]	R/W	00000	Analog gain control: 00000: 0db (29.5Vp/FS) 00001: -0.5dB 00010: -1dB 11111: -15.5dB

9.2.1.3 AMP_CTRL3 (Page 0, Offset=3h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

reserved	ana_gain_ch2[4:0]
R/W	R/W

Bit	Field	Type	Reset	Description
7:5	reserved	R/W	000	These bits are reserved
4:0	ana_gain_ch2[4:0]	R/W	00000	00000: 0dB (29.5Vp/FS) 00001:-0.5dB 11111: -15.5db

9.2.1.4 AMP_CTRL4 (Page 0,Offset=4h) [Reset=0x00]

7	6	5	4	3	2	1	0
reserved			ana_gain_ch3[4:0]				
R/W			R/W				

Bit	Field	Type	Reset	Description
7:5	reserved	R/W	000	These bits are reserved
4:0	ana_gain_ch3[4:0]	R/W	00000	00000: 0dB (29.5Vp/FS) 00001:-0.5dB 11111: -15.5db

9.2.1.5 AMP_CTRL5 (Page 0,Offset=5h) [Reset=0x00]

7	6	5	4	3	2	1	0
reserved			ana_gain_ch4[4:0]				
R/W			R/W				

Bit	Field	Type	Reset	Description
7:5	reserved	R/W	000	These bits are reserved
4:0	ana_gain_ch4[4:0]	R/W	00000	00000: 0dB (29.5Vp/FS) 00001:-0.5dB 11111: -15.5db

9.2.1.6 ANA_CTRL1 (Page 0,Offset=6h) [Reset=0x00]

7	6	5	4	3	2	1	0
ana_ctrl1[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:5	bw_sel[2:0]	R/W	000	Class-d modulation bandwidth selection: 000:155K 001:180K 010:200K 011:235K 100:270K 101:320K 110: 400K 111: 460K
4:3	reserved	R/W	00	These bits are reserved
2:1	psave[1:0]	R/W	00	Damp bias current setting:

Bit	Field	Type	Reset	Description
				00: 1X 01:0.66X 10:0.5X 11:0.33X
0	reserved	R/W	0	This bit is reserved

9.2.1.7 DIG_STATE_CTRL1 (Page 0,Offset=8h) [Reset=0x00]

7	6	5	4	3	2	1	0
rst_reg	rst_mod	force_rst_mode	reserved		otw_global_sel[2:0]		
R/W	R/W	R/W	R/W		R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	rst_reg	R/W	0	Reset reg_map
6	rst_mod	R/W	0	Reset signal path
5	force_rst_mode	R/W	0	Force reset signal path, back to DSP_BOOT
4:3	reserved	R/W	00	These bits are reserved
2:0	otw_global_sel[2:0]	R/W	000	Device global temperature warning threshold: 0: 95C 1: 105C 2: 115C 3: 125C 4: 135C 5: 145C 6: 155C 7: 160C

9.2.1.8 DIG_STATE_CTRL2 (Page 0,Offset=9h) [Reset=0x00]

7	6	5	4	3	2	1	0
reserved	otw_ch1_sel[2:0]			mute_ch1	ctrl_state_ch1[2:0]		
R/W	R/W			R/W	R/W		

Bit	Field	Type	Reset	Description
7	reserved	R/W	0	This bit is reserved
6:4	otw_ch1_sel[2:0]	R/W	000	Channel1 temperature warning threshold: 0: 95C 1: 105C 2: 115C 3: 125C 4: 135C 5: 145C 6: 155C 7: 170C(OTSD)
3	mute_ch1	R/W	0	Channel1 mute control: 0: Unmute CH1 1: Mute CH
2:0	ctrl_state_ch1[2:0]	R/W	000	Channel 1 working state control: 0: deep_sleep 1: sleep 2: dc_diag_manual 3: ac_diag_manual 4: hiz 5: play

9.2.1.9 DIG_STATE_CTRL3 (Page 0,Offset=Ah) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

reserved	otw_ch2_sel[2:0]	mute_ch2	ctrl_state_ch2[2:0]
R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	reserved	R/W	0	This bit is reserved
6:4	otw_ch2_sel[2:0]	R/W	000	0: 95C 1: 105C 2: 115C 3: 125C 4: 135C 5: 145C 6: 155C 7: 170C(OTSD)
3	mute_ch2	R/W	0	0: Unmute ch2 1: Mute ch2
2:0	ctrl_state_ch2[2:0]	R/W	000	0: deep_sleep 1: sleep 2: dc_diag_manual 3: ac_diag_manual 4: hiz 5: play

9.2.1.10 DIG_STATE_CTRL4 (Page 0,Offset=Bh) [Reset=0x00]

7	6	5	4	3	2	1	0
reserved	otw_ch3_sel[2:0]			mute_ch3	ctrl_state_ch3[2:0]		
R/W	R/W			R/W	R/W		

Bit	Field	Type	Reset	Description
7	reserved	R/W	0	This bit is reserved
6:4	otw_ch3_sel[2:0]	R/W	000	0: 95C 1: 105C 2: 115C 3: 125C 4: 135C 5: 145C 6: 155C 7: 170C(OTSD)
3	mute_ch3	R/W	0	0: Unmute ch3 1: Mute ch3
2:0	ctrl_state_ch3[2:0]	R/W	000	0: deep_sleep 1: sleep 2: dc_diag_manual 3: ac_diag_manual 4: hiz 5: play

9.2.1.11 DIG_STATE_CTRL5 (Page 0,Offset=Ch) [Reset=0x00]

7	6	5	4	3	2	1	0
reserved	otw_ch4_sel[2:0]			mute_ch4	ctrl_state_ch4[2:0]		
R/W	R/W			R/W	R/W		

Bit	Field	Type	Reset	Description
7	reserved	R/W	0	This bit is reserved
6:4	otw_ch4_sel[2:0]	R/W	000	0: 95C 1: 105C 2: 115C 3: 125C 4: 135C

Bit	Field	Type	Reset	Description
				5: 145C 6: 155C 7: 170C(OTSD)
3	mute_ch4	R/W	0	0: Unmute ch4 1: Mute ch4
2:0	ctrl_state_ch4[2:0]	R/W	000	0: deep_sleep 1: sleep 2: dc_diag_manual 3: ac_diag_manual 4: hiz 5: play

9.2.1.12 DSP_CTRL1 (Page 0, Offset=Dh) [Reset=0x00]

7	6	5	4	3	2	1	0
dsp_ctrl [7:0]							
R/W							

Bit	Field	Type	Reset	Description
7	dsp_ctrl1 [7:0]	R/W	00000000	bit[1:0]: 10/11, bypass eq, bypass real-time open load detection; 01: bypass real-time open load detection, enable eq; 00: enable real-time open load detection, bypass eq Bit[2] 0: Enable real-time short load detection ; 1: bypass real-time short load detection. Bit[3] 0: enable lookahead ; 1: bypass lookahead. Bit[4] 0: enable clipping detection ; 1: bypass clipping detection. Bit[5] 0: enable Class-H control ; 1: bypass Class-H control. Bit[6] 0: enable IIR filter as interpolation filter ; 1: bypass IIR filter as interpolation filter. Bit[7] NA

9.2.1.13 DIG_I2S_DATA_FORMAT1 (Page 0, Offset=10h) [Reset=0x02]

7	6	5	4	3	2	1	0
i2s_input_44k	det_44k_en	i2s_data_format[1:0]		i2s_lrck_pulse[1:0]		i2s_word_length[1:0]	
R/W	R/W	R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7	i2s_input_44k	R/W	0	0: disable 44k bclk mode 1: enable 44K bclk mode, ramp
6	det_44k_en	R/W	0	0: disable 1: enable 44K/88K clk det
5:4	i2s_data_format[1:0]	R/W	00	0: I2S , 1: LJ, 2: RJ, 3: DSP
3:2	i2s_lrck_pulse[1:0]	R/W	00	01: lrclk pulse < 8 sclk
1:0	i2s_word_length[1:0]	R/W	10	00:16bit 01:20bit 10:24bit 11:32bit

9.2.1.14 DIG_I2S_DATA_FORMAT2 (Page 0, Offset=11h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

i2s_shift_ch1[7:0]

R/W

Bit	Field	Type	Reset	Description
7:0	i2s_shift_ch1[7:0]	R/W	00000000	00000000 : offset = 0 00000001: offset = 1 11111111: offset = 512

9.2.1.15 DIG_I2S_DATA_FORMAT3 (Page 0,Offset=12h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

i2s_shift_ch2[7:0]

R/W

Bit	Field	Type	Reset	Description
7:0	i2s_shift_ch2[7:0]	R/W	00000000	00000000 : offset = 0 00000001: offset = 1 11111111: offset = 512

9.2.1.16 DIG_I2S_DATA_FORMAT4 (Page 0,Offset=13h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

i2s_shift_ch3[7:0]

R/W

Bit	Field	Type	Reset	Description
7:0	i2s_shift_ch3[7:0]	R/W	00000000	00000000 : offset = 0 00000001: offset = 1 11111111: offset = 512

9.2.1.17 DIG_I2S_DATA_FORMAT5 (Page 0,Offset=14h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

i2s_shift_ch4[7:0]

R/W

Bit	Field	Type	Reset	Description
7:0	i2s_shift_ch4[7:0]	R/W	00000000	00000000 : offset = 0 00000001: offset = 1 11111111: offset = 512

9.2.1.18 DIG_TARGET_VOL_CH1 (Page 0,Offset=15h) [Reset=0xCF]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

target_vol_ch1[7:0]

R/W

Bit	Field	Type	Reset	Description
7:0	target_vol_ch1[7:0]	R/W	11001111	0.5 db per step 00000000: -127.5dB 00000001: -127dB 11001111: 0dB 11111111: 24dB

9.2.1.19 DIG_TARGET_VOL_CH2 (Page 0,Offset=16h) [Reset=0xCF]

7	6	5	4	3	2	1	0
target_vol_ch2[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	target_vol_ch2[7:0]	R/W	11001111	0.5 db per step 00000000: -127.5dB 00000001: -127dB 11001111: 0dB 11111111: 24dB

9.2.1.20 DIG_TARGET_VOL_CH3 (Page 0,Offset=17h) [Reset=0xCF]

7	6	5	4	3	2	1	0
target_vol_ch3[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	target_vol_ch3[7:0]	R/W	11001111	0.5 db per step 00000000: -127.5dB 00000001: -127dB 11001111: 0dB 11111111: 24dB

9.2.1.21 DIG_TARGET_VOL_CH4 (Page 0,Offset=18h) [Reset=0xCF]

7	6	5	4	3	2	1	0
target_vol_ch4[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	target_vol_ch4[7:0]	R/W	11001111	0.5 db per step 00000000: -127.5dB 00000001: -127dB 11001111: 0dB 11111111: 24dB

9.2.1.22 DIG_I2S_BAK2 (Page 0,Offset=1Ah) [Reset=0x01]

7	6	5	4	3	2	1	0
i2s_shift_ch4_high	i2s_shift_ch3_high	i2s_shift_ch2_high	i2s_shift_ch1_high	Reserved			
R/W	R/W	R/W	R/W	R/W			

Bit	Field	Type	Reset	Description
7	i2s_shift_ch4_high	R/W	0	MSB of i2s_shift_ch4
6	i2s_shift_ch3_high	R/W	0	MSB of i2s_shift_ch3
5	i2s_shift_ch2_high	R/W	0	MSB of i2s_shift_ch2
4	i2s_shift_ch1_high	R/W	0	MSB of i2s_shift_ch1
3:0	Reserved	R/W	0001	These bits are reserved

9.2.1.23 DIG_SS_CTRL (Page 0,Offset 1Fh) [Reset=0x20]

7	6	5	4	3	2	1	0
Reserved					ramp_mode	ss_rdm_en	ss_tri_en
R/W					R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:3	Reserved	R/W	00000	This bit is reserved
2	ramp_mode	R/W	0	0: open loop 1: close loop,
1	ss_rdm_en	R/W	0	0: disable random ramp ss 1: enable random ramp ss
0	ss_tri_en	R/W	0	0: disable triangle ramp ss 1: enable triangle ramp ss

9.2.1.24 DIG_RTLDG_OL_CTRL (Page 0,Offset=23h) [Reset=0xdd]

7	6	5	4	3	2	1	0
sl_det_window[2:0]			sl_det_en	ol_det_window[2:0]			ol_det_en
R/W			R/W	R/W			R/W

Bit	Field	Type	Reset	Description
7:5	sl_det_window[2:0]	R/W	110	0: 100us 1: 200us 2: 400us 3: 800us 4: 1.6ms 5: 3.2ms 6: 6.4ms 7: 12.8ms
4	sl_det_en	R/W	1	0: disable real-time short-load detection 1: enable real-time short-load detection
3:1	ol_det_window[2:0]	R/W	110	0: 1.6ms 1: 3.2ms 2: 6.2ms 3: 12.5ms 4: 25ms 5: 50ms 6: 100ms 7: 200ms
0	ol_det_en	R/W	1	0: disable real-time open-load detection 1: enable real-time open-load detection

9.2.1.25 DIG_MISC_CTRL2 (Page 0,Offset=25h) [Reset=0x08]

7	6	5	4	3	2	1	0
misc_ctrl2[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7	Ldo_5v_disable	R/W	0	0: ldo_5v_enable 1: ldo_5v_disable
6:3	Reserved	R/W	00	These bits are reserved
2	Rtldg_sl_sequence_disable	R/W	0	0: once real-time short load happens, amplifier outputs stop switching 1: once real-time short load happens, amplifier outputs keep switching
1	rtldg_ol_sequence_disable	R/W	0	0: once real-time open load happens, amplifier outputs stop switching 1: once real-time open load happens, amplifier outputs keep switching
0	Reserved	R/W	0	This bit is reserved

9.2.1.26 DIG_PTSNS_CTRL (Page 0,Offset=26h) [Reset=0x03]

7	6	5	4	3	2	1	0
Reserved			otsd_auto_rec_en	Reserved	reg_ptsns_latch_data	reg_tsns_en	reg_psns_en
R/W			R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:5	reserved	R/W	0	These bits are reserved
4	otsd_auto_rec_en	R/W	0	0: disable auto-recovery when temperature is lower than otsd threshold 1: enable auto-recovery when temperature is lower than otsd threshold
3	reserved	R/W	0	This bit is reserved
2	reserved	R/W	0	This bit is reserved
1	tsns_en	R/W	1	0: disable temperature sense 1: enable temperature sense
0	psns_en	R/W	1	0: disable pvdd sense 1: enable pvdd sense

9.2.1.27 DIG_ANA_CTRL_BAK (Page 0,Offset=27h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved							clip_mode
R/W							R/W

Bit	Field	Type	Reset	Description
7:1	Reserved	R/W	0000000	These bits are reserved
0	clip_mode	R/W	0	Clipping detection method 0: use digital clip 1: use analog clip;

9.2.1.28 ANA_CTRL3 (Page 0, Offset=28h) [Reset=0x00]

7	6	5	4	3	2	1	0
OL_DET_DISABLE	LDO5V_CTRL<2:0>			PVDD_UV7V_SEL	Reserved		
R/W	R/W			R/W	R/W		

Bit	Field	Type	Reset	Description
7	OL_DET_DISABLE	R/W	0	Disable Real time open load detection : 0: enable 1: disable
6:4	ldo5v_ctrl[2:0]	R/W	000	AVDD, GVDD output voltage control: 000: 5.06 001: 5.26 010: 5.46 011: 5.66 100: 4.26 101: 4.46 110: 4.66 111: 4.86
3	pvdd_uv7v_sel	R/W	0	Pvdd uv detection threshold 7V enable 0: 4.5V 1: 7V
2:0	reserved	R/W	000	This bit is reserved

9.2.1.29 DIG_DC_DIAG_SL_DET_THRESHOLD1 (Page 0, Offset=2Ah) [Reset=0x36]

7	6	5	4	3	2	1	0
sl_det_threshold_low_ch1[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	sl_det_threshold_low_ch1[7:0]	R/W	00110110	Short load detection threshold low 8 bits of channel 1 [7:0] of sl_det_threshold_ch1[9:0]

9.2.1.30 DIG_DC_DIAG_SL_DET_THRESHOLD2 (Page 0, Offset=2Bh) [Reset=0x36]

7	6	5	4	3	2	1	0
sl_det_threshold_low_ch2[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	sl_det_threshold_low_ch2[7:0]	R/W	00110110	[7:0] of sl_det_threshold_ch2[9:0]

9.2.1.31 DIG_DC_DIAG_SL_DET_THRESHOLD3 (Page 0, Offset=2Ch) [Reset=0x36]

7	6	5	4	3	2	1	0
sl_det_threshold_low_ch3[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	sl_det_threshold_low_ch3[7:0]	R/W	00110110	[7:0] of sl_det_threshold_ch3[9:0]

9.2.1.32 DIG_DC_DIAG_SL_DET_THRESHOLD4 (Page 0,Offset=2Dh) [Reset=0x36]

7	6	5	4	3	2	1	0
sl_det_threshold_low_ch4[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	sl_det_threshold_low_ch4[7:0]	R/W	00110110	[7:0] of sl_det_threshold_ch4[9:0]

9.2.1.33 DIG_DC_DIAG_SL_DET_THRESHOLD5 (Page 0,Offset=2Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_threshold_high_ch4[1:0]		sl_det_threshold_high_ch3[1:0]		sl_det_threshold_high_ch2[1:0]		sl_det_threshold_high_ch1[1:0]	
R/W		R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7:6	sl_det_threshold_high_ch4[1:0]	R/W	00	Short load detection threshold high 2 bits of channel1: [9:8] of sl_det_threshold_ch1[9:0]
5:4	sl_det_threshold_high_ch3[1:0]	R/W	00	[9:8] of sl_det_threshold_ch2[9:0]
3:2	sl_det_threshold_high_ch2[1:0]	R/W	00	[9:8] of sl_det_threshold_ch3[9:0]
1:0	sl_det_threshold_high_ch1[1:0]	R/W	00	[9:8] of sl_det_threshold_ch4[9:0]

9.2.1.34 DIG_DC_DIAG_CTRL1 (Page 0,Offset=30h) [Reset=0x15]

7	6	5	4	3	2	1	0
s2ps2g_post_dec_factor[2:0]		lineout_repeat_en		ldg_ac_loop_back_en	ac_diag_en	dc_diag_abort	dc_diag_en
R/W		R/W		R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:5	s2ps2g_post_dec_factor[2:0]	R/W	000	2 nd decimation filter rate: 000:32x, 001:64x, 010:128x, 011/100/101:256x, 110: 512x, 111:2x
4	lineout_repeat_en	R/W	1	0: check lineout 1 times before report fault 1: check lineout 2 times before report fault
3	ldg_ac_loop_back_en	R/W	0	0: disable ac load detection loop back mode 1: enable ac load detection loop back mode
2	ac_diag_en	R/W	1	0: disable ac diagnostic check 1: enable ac diagnostic check
1	dc_diag_abort	R/W	0	0: run dc-diagnostic normally 1: force skip dc diagnostic check, stop the dc diagnostic check even the dc diagnostic on-going
0	dc_diag_en	R/W	1	0: disable dc diagnostic check 1: enable dc diagnostic check

9.2.1.35 DIG_DC_DIAG_CTRL2 (Page 0,Offset=31h) [Reset=0x77]

7	6	5	4	3	2	1	0
ch2_lineout_en	ch2_slol_en	ch2_s2g_en	ch2_s2p_en	ch1_lineout_en	ch1_slol_en	ch1_s2g_en	ch1_s2p_en
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	ch2_lineout_en	R/W	0	0: disable ch2 lineout check 1: enable ch2 lineout check
6	ch2_slol_en	R/W	1	0: disable ch2 short load/open load check 1: enable ch2 short load/open load check
5	ch2_s2g_en	R/W	1	0: disable ch2 short to ground check 1: enable ch2 short to ground check
4	ch2_s2p_en	R/W	1	0: disable ch2 short to power check 1: enable ch2 short to power check
3	ch1_lineout_en	R/W	0	0: disable ch1 lineout check 1: enable ch1 lineout check
2	ch1_slol_en	R/W	1	0: disable ch1 short load/open load check 1: enable ch1 short load/open load check
1	ch1_s2g_en	R/W	1	0: disable ch1 short to ground check 1: enable ch1 short to ground check
0	ch1_s2p_en	R/W	1	0: disable ch1 short to power check 1: enable ch1 short to power check

9.2.1.36 DIG_DC_DIAG_CTRL3 (Page 0, Offset=32h) [Reset=0x77]

7	6	5	4	3	2	1	0
ch4_lineout_en	ch4_slol_en	ch4_s2g_en	ch4_s2p_en	ch3_lineout_en	ch3_slol_en	ch3_s2g_en	ch3_s2p_en
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	ch4_lineout_en	R/W	0	0: disable ch4 lineout check 1: enable ch4 lineout check
6	ch4_slol_en	R/W	1	0: disable ch4 short load/open load check 1: enable ch4 short load/open load check
5	ch4_s2g_en	R/W	1	0: disable ch4 short to ground check 1: enable ch4 short to ground check
4	ch4_s2p_en	R/W	1	0: disable ch4 short to power check 1: enable ch4 short to power check
3	ch3_lineout_en	R/W	0	0: disable ch3 lineout check 1: enable ch3 lineout check
2	ch3_slol_en	R/W	1	0: disable ch3 short load/open load check 1: enable ch3 short load/open load check
1	ch3_s2g_en	R/W	1	1: disable ch3 short to ground check 1: enable ch3 short to ground check
0	ch3_s2p_en	R/W	1	0: disable ch3 short to power check 1: enable ch3 short to power check

9.2.1.37 DIG_DC_DIAG_AC_REPEAT (Page 0, Offset=33h) [Reset=0x50]

7	6	5	4	3	2	1	0
ac_repeat_threshold[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	ac_repeat_threshold[7:0]	R/W	01010000	ac load detection repeat time

9.2.1.38 DIG_DC_DIAG_AC_FREQ1 (Page 0, Offset=34h) [Reset=0x99]

7	6	5	4	3	2	1	0
freq_int_low[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	freq_int_low[7:0]	R/W	10011001	[7:0] of freq_int, ac sin_freq=3072/(nco_max/freq_int)

9.2.1.39 DIG_DC_DIAG_AC_FREQ2 (Page 0,Offset=35h) [Reset=0x99]

7	6	5	4	3	2	1	0
freq_int_mid[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	freq_int_mid[7:0]	R/W	10011001	[15:8] of freq_int

9.2.1.40 DIG_DC_DIAG_AC_FREQ3 (Page 0,Offset=36h) [Reset=0x01]

7	6	5	4	3	2	1	0
freq_int_high[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	freq_int_high[7:0]	R/W	00000001	[23:16] of freq_int

9.2.1.41 DIG_DC_DIAG_S2PS2G_STI (Page 0,Offset=3Ah) [Reset=0xc8]

7	6	5	4	3	2	1	0
s2ps2g_sti[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	s2ps2g_sti[7:0]	R/W	11001000	Short to power and short to ground detection DAC output current setting: 200: 1mA stimulus in s2p s2g test 5uA/LSB

9.2.1.42 DIG_DC_DIAG_SL0L_STI (Page 0,Offset=3Bh) [Reset=0xdc]

7	6	5	4	3	2	1	0
sl0l_sti[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	sl0l_sti[7:0]	R/W	11011100	Short load and open load dac output current setting: 220: 10mA stimulus in sl ol test 45.4uA/LSB

9.2.1.43 DIG_DC_DIAG_LINEOUT_STI (Page 0,Offset=3Ch) [Reset=0x32]

7	6	5	4	3	2	1	0
lineout_sti[7:0]							

R/W

Bit	Field	Type	Reset	Description
7:0	lineout_sti[7:0]	R/W	00110010	Lineout detection dac output current setting: 200: 1mA stimulus in lineout test 5uA/LSB

9.2.1.44 DIG_DC_DIAG_S2P_DET_THRESHOLD1 (Page 0,Offset=3Dh) [Reset=0xC0]

7	6	5	4	3	2	1	0
s2p_det_threshold_low[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	s2p_det_threshold_low[7:0]	R/W	11000000	Short to power threshold low 8bits [7:0] of s2p_det_threshold

9.2.1.45 DIG_DC_DIAG_S2P_DET_THRESHOLD2 (Page 0,Offset=3Eh) [Reset=0x03]

7	6	5	4	3	2	1	0
Reserved		s2p_det_threshold_high[5:0]					
R/W		R/W					

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	These bits are reserved
5:0	s2p_det_threshold_high[5:0]	R/W	000011	Short to power threshold high 5 bit [13:8] of s2p_det_threshold

9.2.1.46 DIG_DC_DIAG_S2G_DET_THRESHOLD1 (Page 0,Offset=3Fh) [Reset=0xC0]

7	6	5	4	3	2	1	0
s2g_det_threshold_low[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	s2g_det_threshold_low[7:0]	R/W	11000000	Short to ground threshold low 8 bits setting: [7:0] of s2g_det_threshold

9.2.1.47 DIG_DC_DIAG_S2G_DET_THRESHOLD2 (Page 0,Offset=40h) [Reset=0x3C]

7	6	5	4	3	2	1	0
Reserved		s2g_det_threshold_high[5:0]					
R/W		R/W					

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	
5:0	s2g_det_threshold_high[5:0]	R/W	111100	Short to ground high 5 bits threshold setting: [13:8] of s2p_det_threshold

9.2.1.48 DIG_DC_DIAG_SLOL_DET_GAIN (Page 0, Offset=41h) [Reset=0xFF]

7	6	5	4	3	2	1	0
slo_det_gain_ch4[1:0]		slo_det_gain_ch3[1:0]		slo_det_gain_ch2[1:0]		slo_det_gain_ch1[1:0]	
R/W		R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7:6	slo_det_gain_ch4[1:0]	R/W	11	Short load and open load adc gain setting: 00: 1x, 01:16x, 10:4x, 11:8x Channel 4 adc gain in DC_LDG short load and open load test
5:4	slo_det_gain_ch3[1:0]	R/W	11	00: 1x, 01:16x, 10:4x, 11:8x Channel 3 adc gain in DC_LDG short load and open load test
3:2	slo_det_gain_ch2[1:0]	R/W	11	00: 1x, 01:16x, 10:4x, 11:8x Channel 4 adc gain in DC_LDG short load and open load test
1:0	slo_det_gain_ch1[1:0]	R/W	11	00: 1x, 01:16x, 10:4x, 11:8x Channel 1 adc gain in DC_LDG short load and open load test

9.2.1.49 DIG_DC_DIAG_OL_DET_THRESHOLD1 (Page 0, Offset=43h) [Reset=0x64]

7	6	5	4	3	2	1	0
ol_det_threshold_low[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	ol_det_threshold_low[7:0]	R/W	01100100	Open load detection threshold low 8 bits setting: [7:0] of ol_det_threshold[13:0]

9.2.1.50 DIG_DC_DIAG_OL_DET_THRESHOLD2 (Page 0, Offset=44h) [Reset=0x19]

7	6	5	4	3	2	1	0
Reserved		ol_det_threshold_high[5:0]					
R/W		R/W					

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	
5:0	ol_det_threshold_high[5:0]	R/W	011001	Open load detection threshold high 5 bits setting: [13:8] of ol_det_threshold[13:0]

9.2.1.51 DIG_DC_DIAG_LINEOUT_DET_THRESHOLD1 (Page 0, Offset=45h) [Reset=0x00]

7	6	5	4	3	2	1	0
lineout_det_threshold_low[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	lineout_det_threshold_low[7:0]	R/W	00000000	Lineout detection threshold low 8 bits setting: [7:0] of lineout_det_threshold[13:0]

9.2.1.52 DIG_DC_DIAG_LINEOUT_DET_THRESHOLD2 (Page 0,Offset=46h) [Reset=0x0C]

7	6	5	4	3	2	1	0
Reserved		lineout_det_threshold_high[5:0]					
R/W		R/W					

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	These bits are reserved
5:0	lineout_det_threshold_high[5:0]	R/W	01100	Linedout detection threshold high 5 bits setting: [13:8] of lineout_det_threshold[13:0]

9.2.1.53 DIG_DC_DIAG_CTRL3 (Page 0,Offset=47h) [Reset=0x1b]

7	6	5	4	3	2	1	0
lineout_dac_settle_time	olsl_dac_settle_time	s2pg_dac_settle_time	reg_slol_pre_dec_factor[1:0]		reg_slol_post_dec_factor[2:0]		
R/W	R/W	R/W	R/W		R/W		

Bit	Field	Type	Reset	Description
7	lineout_dac_settle_time	R/W	0	0: 40ms, 1:80ms
6	olsl_dac_settle_time	R/W	0	0: 20ms, 1:40ms
5	s2pg_dac_settle_time	R/W	0	0: 20ms, 1:40ms
4:3	reg_slol_pre_dec_factor[1:0]	R/W	11	Decimation 00: 128, 01:256, 10:512, 11:1024
2:0	reg_slol_post_dec_factor[2:0]	R/W	011	Decimation 000:32x, 001:64x, 010:128x, 011-101:256x, 110: 512x, 111:2x

9.2.1.54 DIG_DC_DET_FACTOR2 (Page 0,Offset=48h) [Reset=0x1b]

7	6	5	4	3	2	1	0
Reserved			reg_lineout_pre_dec_factor[1:0]		reg_lineout_post_dec_factor[2:0]		
R/W			R/W		R/W		

Bit	Field	Type	Reset	Description
7:5	Reserved	R/W	000	These bits are reserved
4:3	reg_lineout_pre_dec_factor[1:0]	R/W	11	Decimation 00: 128, 01:256, 10:512, 11:1024
2:0	reg_lineout_post_dec_factor[2:0]	R/W	011	Decimation 000:32x,

Bit	Field	Type	Reset	Description
				001:64x, 010:128x, 011-101:256x , 110: 512x, 111:2x

9.2.1.55 DIG_DC_DIAG_RPT1 (Page 0,Offset=49h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved	ch1_ac_diag_done	ch1_dc_diag_done	ch1_lineout_fault	ch1_ol_fault	ch1_sl_fault	ch1_s2g_fault	ch1_s2p_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	Reserved	RO	0	This bit is reserved
6	ch1_ac_diag_done	RO	0	0:ch1 ac diagnostic is on-going 1:Ch1 ac_diag is done
5	ch1_dc_diag_done	RO	0	0:ch1 dc diagnostic is on-going 1:ch1 dc_diag is done and there is not fault
4	ch1_lineout_fault	RO	0	0:ch1_linout diagnostic no fault 1:ch1_lineout_fault
3	ch1_ol_fault	RO	0	0: ch1 open load no fault 1: ch1 open load fault
2	ch1_sl_fault	RO	0	0: ch1 short load no fault 1: ch1 short load fault
1	ch1_s2g_fault	RO	0	0:ch1 short to ground no fault 1:ch1 short to ground fault
0	ch1_s2p_fault	RO	0	0:ch1 short to pvdd no fault 1:ch1 short to pvdd fault

9.2.1.56 DIG_DC_DIAG_RPT2 (Page 0,Offset=4Ah) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved	Ch2_ac_diag_done	Ch2_dc_diag_done	Ch2_lineout_fault	Ch2_ol_fault	Ch2_sl_fault	Ch2_s2g_fault	Ch2_s2p_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	Reserved	RO	0	This bit is reserved
6	Ch2_ac_diag_done	RO	0	0:ch2 ac diagnostic is on-going 1:Ch2 ac_diag is done
5	Ch2_dc_diag_done	RO	0	0:ch2 dc diagnostic is on-going 1:ch2 dc_diag is done and there is not fault
4	Ch2_lineout_fault	RO	0	0:ch2_linout diagnostic no fault 1:ch2_lineout_fault
3	Ch2_ol_fault	RO	0	0: ch2 open load no fault 1: ch2 open load fault
2	Ch2_sl_fault	RO	0	0: ch2 short load no fault 1: ch2 short load fault
1	Ch2_s2g_fault	RO	0	0:ch2 short to ground no fault 1:ch2 short to ground fault
0	Ch2_s2p_fault	RO	0	0:ch2 short to pvdd no fault 1:ch2 short to pvdd fault

9.2.1.57 DIG_DC_DIAG_RPT3 (Page 0,Offset=4Bh) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved	Ch3_ac_diag_done	Ch3_dc_diag_done	Ch3_lineout_fault	Ch3_ol_fault	Ch3_sl_fault	Ch3_s2g_fault	Ch3_s2p_fault

RO	RO	RO	RO	RO	RO	RO	RO
----	----	----	----	----	----	----	----

Bit	Field	Type	Reset	Description
7	Reserved	RO	0	This bit is reserved
6	Ch3_ac_diag_done	RO	0	0:ch3 ac diagnostic is on-going 1:Ch3 ac_diag is done
5	Ch3_dc_diag_done	RO	0	0:ch3 dc diagnostic is on-going 1:ch3 dc_diag is done and there is not fault
4	Ch3_lineout_fault	RO	0	0:ch3_lineout diagnostic no fault 1:ch3_lineout_fault
3	Ch3_ol_fault	RO	0	0: ch3 open load no fault 1: ch3 open load fault
2	Ch3_sl_fault	RO	0	0: ch3 short load no fault 1: ch3 short load fault
1	Ch3_s2g_fault	RO	0	0:ch3 short to ground no fault 1:ch3 short to ground fault
0	Ch3_s2p_fault	RO	0	0:ch3 short to pvdd no fault 1:ch3 short to pvdd fault

9.2.1.58 DIG_DC_DIAG_RPT3 (Page 0, Offset=4Ch) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved	Ch4_ac_diag_done	Ch4_dc_diag_done	Ch4_lineout_fault	Ch4_ol_fault	Ch4_sl_fault	Ch4_s2g_fault	Ch4_s2p_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	Reserved	RO	0	This bit is reserved
6	Ch4_ac_diag_done	RO	0	0:ch4 ac diagnostic is on-going 1:Ch4 ac_diag is done
5	Ch4_dc_diag_done	RO	0	0:ch4 dc diagnostic is on-going 1:ch4 dc_diag is done and there is not fault
4	Ch4_lineout_fault	RO	0	0:ch4_lineout diagnostic no fault 1:ch4_lineout_fault
3	Ch4_ol_fault	RO	0	0: ch4 open load no fault 1: ch4 open load fault
2	Ch4_sl_fault	RO	0	0: ch4 short load no fault 1: ch4 short load fault
1	Ch4_s2g_fault	RO	0	0:ch4 short to ground no fault 1:ch4 short to ground fault
0	Ch4_s2p_fault	RO	0	0:ch4 short to pvdd no fault 1:ch4 short to pvdd fault

9.2.1.59 DIG_DC_DIAG_RPT5 (Page 0, Offset=4Dh) [Reset=0x00]

7	6	5	4	3	2	1	0
ch2_s2pp_fault	ch2_s2pn_fault	ch2_s2gp_fault	ch2_s2gn_fault	ch1_s2pp_fault	ch1_s2pn_fault	ch1_s2gp_fault	ch1_s2gn_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	ch2_s2pp_fault	RO	0	0: normal 1: Ch2 s2p fault in outp
6	ch2_s2pn_fault	RO	0	0: normal 1:ch2 s2p fault in outn
5	ch2_s2gp_fault	RO	0	0: normal 1: ch2 s2g fault in outp
4	ch2_s2gn_fault	RO	0	0: normal 1: ch2 s2g fault in outn
3	ch1_s2pp_fault	RO	0	0: normal 1: ch1 s2p fault in outp
2	ch1_s2pn_fault	RO	0	0: normal

Bit	Field	Type	Reset	Description
1	ch1_s2gp_fault	RO	0	0: normal 1: ch1 s2g fault in outn
0	ch1_s2gn_fault	RO	0	0: normal 1: ch1 s2g fault in outn

9.2.1.60 DIG_DC_DIAG_RPT6 (Page 0,Offset=4Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
ch4_s2pp_fault	ch4_s2pn_fault	ch4_s2gp_fault	ch4_s2gn_fault	ch3_s2pp_fault	ch3_s2pn_fault	ch3_s2gp_fault	ch3_s2gn_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	ch4_s2pp_fault	RO	0	0: normal 1: ch4 s2p fault in outp
6	ch4_s2pn_fault	RO	0	0: normal 1: ch4 s2p fault in outn
5	ch4_s2gp_fault	RO	0	0: normal 1: ch4 s2g fault in outp
4	ch4_s2gn_fault	RO	0	0: normal 1: ch4 s2g fault in outn
3	ch3_s2pp_fault	RO	0	0: normal 1: ch3 s2p fault in outp
2	ch3_s2pn_fault	RO	0	0: normal 1: ch3 s2p fault in outn
1	ch3_s2gp_fault	RO	0	0: normal 1: ch3 s2g fault in outp
0	ch3_s2gn_fault	RO	0	0: normal 1: ch3 s2g fault in outn

9.2.1.61 DIG_DC_DIAG_RPT7 (Page 0,Offset=4Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_data_low_ch1[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	sl_det_data_low_ch1[7:0]	RO	0	Channel 1 Short load detection result low 8 bits report [7:0] of ch1 sl det data

9.2.1.62 DIG_DC_DIAG_RPT8 (Page 0,Offset=50h) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_data_low_ch2[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	sl_det_data_low_ch2[7:0]	RO	0	Channel 2 Short load detection low 8 bits result report [7:0] of ch2 sl det data

9.2.1.63 DIG_DC_DIAG_RPT9 (Page 0,Offset=51h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

sl_det_data_low_ch3[7:0]

RO

Bit	Field	Type	Reset	Description
7:0	sl_det_data_low_ch3[7:0]	RO	0	Channel 3 Short load detection low 8 bits result report [7:0] of ch3 sl det data

9.2.1.64 DIG_DC_DIAG_RPT10 (Page 0,Offset=52h) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_data_low_ch4[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	sl_det_data_low_ch4[7:0]	RO	0	Channel 4 Short load detection low 8 bits result report [7:0] of ch4 sl det data

9.2.1.65 DIG_DC_DIAG_RPT11 (Page 0,Offset=53h) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_data_high_ch2[3:0]				sl_det_data_high_ch1[3:0]			
RO				RO			

Bit	Field	Type	Reset	Description
7:4	sl_det_data_high_ch2[3:0]	RO	0	Channel 2 Short load detection high 5 bits bits result report [11:8] of ch2 sl det data
3:0	sl_det_data_high_ch1[3:0]	RO	0	Channel 1 Short load detection high 5 bits bits result report [11:8] of ch1 sl det data

9.2.1.66 DIG_DC_DIAG_RPT12 (Page 0,Offset=54h) [Reset=0x00]

7	6	5	4	3	2	1	0
sl_det_data_high_ch4[3:0]				sl_det_data_high_ch3[3:0]			
RO				RO			

Bit	Field	Type	Reset	Description
7:4	sl_det_data_high_ch4[3:0]	RO	0	Channel 4 Short load detection high 5 bits bits result report [11:8] of ch4 sl det data
3:0	sl_det_data_high_ch3[3:0]	RO	0	Channel 3 Short load detection high 5 bits bits result report [11:8] of ch3 sl det data

9.2.1.67 DIG_STATE_RPT_CH12 (Page 0,Offset=60h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved		state_rpt_ch2[2:0]			state_rpt_ch1[2:0]		
RO		RO			RO		

Bit	Field	Type	Reset	Description
7:6	Reserved	RO	0	These bits are reserved
5:3	state_rpt_ch2[2:0]	RO	0	Ch2 status report, 0: deep sleep,

Bit	Field	Type	Reset	Description
				1: sleep, 2: DC_LDG, 3: AC_LDG, 5: hiz, 6: play
2:0	state_rpt_ch1[2:0]	RO	0	Ch1 status report, 0: deep sleep, 1: sleep, 2: DC_LDG, 3: AC_LDG, 5: hiz, 6:play

9.2.1.68 DIG_STATE_RPT_CH34 (Page 0,Offset=61h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved		state_rpt_ch4[2:0]			state_rpt_ch3[2:0]		
RO		RO			RO		

Bit	Field	Type	Reset	Description
7:6	Reserved	RO	0	
5:3	state_rpt_ch4[2:0]	RO	0	Ch4 status report, 0: deep sleep, 1: sleep, 2: DC_LDG, 3: AC_LDG, 5: hiz, 6: play
2:0	state_rpt_ch3[2:0]	RO	0	Ch3 state report, 0: deep sleep, 1: sleep, 2: DC_LDG, 3: AC_LDG, 5: hiz, 6: play

9.2.1.69 DIG_FAULT_RPT1 (Page 0,Offset=62h) [Reset=0x00]

7	6	5	4	3	2	1	0
dc_ch4	dc_ch3	dc_ch2	dc_ch1	oc_ch4	oc_ch3	oc_ch2	oc_ch1
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	dc_ch4	RO	0	0: normal 1: CH4 DC fault
6	dc_ch3	RO	0	0: normal 1: CH3 DC fault
5	dc_ch2	RO	0	0: normal 1: CH2 DC fault
4	dc_ch1	RO	0	0: normal 1: CH1 DC fault
3	oc_ch4	RO	0	0: normal 1: CH4 OCSD fault
2	oc_ch3	RO	0	0: normal 1: CH3 OCSD fault
1	oc_ch2	RO	0	0: normal 1: CH2 OCSD fault
0	oc_ch1	RO	0	0: normal 1: CH1 OCSD fault

9.2.1.70 DIG_FAULT_RPT2 (Page 0,Offset=63h) [Reset=0x00]

7	6	5	4	3	2	1	0
otsd_ch4	otsd_ch3	otsd_ch2	otsd_ch1	otw_ch4	otw_ch3	otw_ch2	otw_ch1
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	otsd_ch4	RO	0	0: normal 1: CH4 OTSD fault
6	otsd_ch3	RO	0	0: normal 1: CH3 OTSD fault
5	otsd_ch2	RO	0	0: normal 1: CH2 OTSD fault
4	otsd_ch1	RO	0	0: normal 1: CH1 OTSD fault
3	otw_ch4	RO	0	0: normal 1: CH4 OTW warning
2	otw_ch3	RO	0	0: normal 1: CH3 OTW warning
1	otw_ch2	RO	0	0: normal 1: CH2 OTW warning
0	otw_ch1	RO	0	0: normal 1: CH1 OTW warning

9.2.1.71 DIG_FAULT_RPT3 (Page 0,Offset=64h) [Reset=0x00]

7	6	5	4	3	2	1	0
clip_ch4	clip_ch3	clip_ch2	clip_ch1	otp_crc_error	bq_wr_error	Reserved	clk_fault
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	clip_ch4	RO	0	0: CH4 no clipping detected. 1: CH4 clip detected
6	clip_ch3	RO	0	0: CH3 no clipping detected 1: CH3 clip detected
5	clip_ch2	RO	0	0: CH2 no clipping detected 1: CH2 clip detected
4	clip_ch1	RO	0	0: CH1 no clipping detected 1: CH1 clip detected
3:0	reserved	RO	0	These bits are reserved
0	clk_fault	RO	0	0: No clock error 1: Clock error detected

9.2.1.72 DIG_FAULT_RPT4 (Page 0,Offset=65h) [Reset=0x00]

7	6	5	4	3	2	1	0
cbc_warning_ch4	cbc_warning_ch3	cbc_warning_ch2	cbc_warning_ch1	cbc_fault_ch4	cbc_fault_ch3	cbc_fault_ch2	cbc_fault_ch1
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	cbc_warning_ch4	RO	0	0: CH3 no CBC warning 1: CH4 cbc warning detected
6	cbc_warning_ch3	RO	0	0: CH3 no CBC warning 1: CH3 cbc warning detected
5	cbc_warning_ch2	RO	0	0: CH2 no CBC warning 1: CH2 cbc warning detected
4	cbc_warning_ch1	RO	0	0: CH1 no CBC warning

Bit	Field	Type	Reset	Description
				1: CH1 cbc warning detected
3	cbc_fault_ch4	RO	0	0: CH4 no CBC fault 1: CH4 cbc fault detected
2	cbc_fault_ch3	RO	0	0: CH3 no CBC fault 1: CH3 cbc fault detected
1	cbc_fault_ch2	RO	0	0: CH2 no CBC fault 1: CH2 cbc fault detected
0	cbc_fault_ch1	RO	0	0: CH1 no CBC fault 1: CH1 cbc fault detected

9.2.1.73 DIG_FAULT_RPT5 (Page 0,Offset=66h) [Reset=0x00]

7	6	5	4	3	2	1	0
oldet_ch4	oldet_ch3	oldet_ch2	oldet_ch1	slidet_ch4	slidet_ch3	slidet_ch2	slidet_ch1
RO	RO	RO	RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7	oldet_ch4	RO	0	0: CH4 no real-time open load fault 1: CH4 real-time open load fault detected
6	oldet_ch3	RO	0	0: CH3 no real-time open load fault 1: CH3 real-time open load fault detected
5	oldet_ch2	RO	0	0: CH2 no real-time open load fault 1: CH2 real-time open load fault detected
4	oldet_ch1	RO	0	0: CH1 no real-time open load fault 1: CH1 real-time open load fault detected
3	slidet_ch4	RO	0	0: CH4 no real-time short load fault 1: CH4 real-time short load fault detected
2	slidet_ch3	RO	0	0: CH3 no real-time short load fault 1: CH3 real-time short load fault detected
1	slidet_ch2	RO	0	0: CH2 no real-time short load fault 1: CH2 real-time short load fault detected
0	slidet_ch1	RO	0	0: CH1 no real-time short load fault 1: CH1 real-time short load fault detected

9.2.1.74 DIG_FAULT_RPT6 (Page 0,Offset=67h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved			gvdd_fault	vbat_ov	vbat_uv	pvdd_ov	pvdd_uv
RO			RO	RO	RO	RO	RO

Bit	Field	Type	Reset	Description
7:5	Reserved	RO	0	This bit is reserved
4	gvdd_fault	RO	0	0: no GVDD fault detected 1: GVDD fault detected
3	vbat_ov	RO	0	0: no VBAT OV fault detected 1: VBAT OV fault detected
2	vbat_uv	RO	0	0: no VBAT UV fault detected 1: VBAT UV fault detected
1	pvdd_ov	RO	0	0: no PVDD OV fault detected 1: PVDD OV fault detected
0	pvdd_uv	RO	0	0: no PVDD UV fault detected 1: PVDD UV fault detected

9.2.1.75 DIG_I2S_CLK_FORMAT_RPT1 (Page 0,Offset=68h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved		bck_ratio_high[1:0]		fs_det[3:0]			
RO		RO		RO			

Bit	Field	Type	Reset	Description
7:6	Reserved	RO	0	These bits are reserved
5:4	bck_ratio_high[1:0]	RO	0	[9:8] of sclk ratio
3:0	fs_det[3:0]	RO	0	0: error, 1:8K, 2:16K, 3:32K, 4: 44K/48K, 5:88K/96K, 6:192K, 7:error

9.2.1.76 DIG_I2S_CLK_FORMAT_RPT2 (Page 0,Offset=69h) [Reset=0x00]

7	6	5	4	3	2	1	0
bck_ratio_low[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	bck_ratio_low[7:0]	R/W	0	[7:0] of sclk ratio

9.2.1.77 DIG_PTSNS_RPT1 (Page 0,Offset=6Ah) [Reset=0x00]

7	6	5	4	3	2	1	0
reg_pvdd[7:0]							
RO							

Bit	Field	Type	Reset	Description
7	reg_pvdd[7:0]	RO	0	PVDD sense data, pvdd= 40/255*data

9.2.1.78 DIG_PTSNS_RPT2 (Page 0,Offset=6Bh) [Reset=0x00]

7	6	5	4	3	2	1	0
reg_temp[7:0]							
RO							

Bit	Field	Type	Reset	Description
7	reg_temp[7:0]	RO	0	Temperature sense data, temp = -57+data, Temperature range : -57C~ 197C

9.2.1.79 DIG_DIEID_RPT (Page 0,Offset=6Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

DIE_ID[7:0]

RO

Bit	Field	Type	Reset	Description
7:0	DIE_ID[7:0]	RO	0	DIE_ID[7:0] = otp_die_ie die_id_metal_opt

9.2.1.80 DIG_XOR_CHECKSUM (Page 0,Offset=7Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
DIG_XOR_CHECKSUM							
RO							

Bit	Field	Type	Reset	Description
7:0	xor_checksum[7:0]	RO	0	

9.2.1.81 DIG_CRC_CHECKSUM (Page 0,Offset=7Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
DIG_CRC_CHECKSUM							
RO							

Bit	Field	Type	Reset	Description
7:0	crc_checksum[7:0]	RO	0	

9.2.2 Page 1 Registers

9.2.2.1 DIG_RTLDG_SLOL_CTRL1 (Page 1,Offset=0Ch) [Reset=0x34]

7	6	5	4	3	2	1	0
Reserved		sl_det_max_window[2:0]			rtldg_sl_skip_cycles_opt[2:0]		
R/W		R/W			R/W		

Bit	Field	Type	Reset	Description
[7:6]	Reserved	R/W	00	
[5:3]	sl_det_max_window[2:0]	R/W	110	
[2:0]	rtldg_sl_skip_cycles_opt[2:0]	R/W	100	

9.2.2.2 DIG_I2S_CLK_FORMAT_LEVEL1 (Page 1,Offset=0Dh) [Reset=0x00]

7	6	5	4	3	2	1	0
bck_ratio_configure[3:0]				fsmode[3:0]			
R/W				R/W			

Bit	Field	Type	Reset	Description
[7:4]	bck_ratio_configure[3:0]	R/W	0000	
[3:0]	fsmode[3:0]	R/W	0000	

9.2.2.3 DIG_I2S_CTRL2_LEVEL1 (Page 1,Offset=0Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved					bck_inv	bck_oe	lrck_oe
R/W					R/W	R/W	R/W

Bit	Field	Type	Reset	Description
[7:3]	Reserved	R/W	00000	These bits are reserved
2	bck_inv	R/W	0	0: non-invert 1: inert
1	Reserved	R/W	0	This bit is reserved
0	Reserved	R/W	0	This bit is reserved

9.2.2.4 DIG_SS_CTRL1_LEVEL1 (Page 1,Offset=2Bh) [Reset=0x10]

7	6	5	4	3	2	1	0
ss_tm_dstep_ctrl_high	ss_tm_ustep_ctrl_high	ss_pre_div_sel	internal_ramp_phase_sel	ramp_phase_sel[1:0]		phase_sync_sel	phase_sync_en
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	ss_tm_dstep_ctrl_high	R/W	0	
6	ss_tm_ustep_ctrl_high	R/W	0	
5	ss_pre_div_sel	R/W	0	
4	internal_ramp_phase_sel	R/W	1	0: 0/90/180/270 1: 0/180/90/270
[3:2]	ramp_phase_sel[1:0]	R/W	00	select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recommended set all device the same RAMP frequency and same spread spectrum. It must be set before driving device into PLAY mode, if this feature is needed 00: 0 01: 45 10: 90 11: 135
1	phase_sync_sel	R/W	0	ramp phase sync sel, 0: gpio sync 1: internal sync
0	phase_sync_en	R/W	0	0: ramp phase sync disable 1: ramp phase sync enable

9.2.2.5 DIG_SS_CTRL2_LEVEL1 (Page 1,Offset=2Ch) [Reset=0x00]

7	6	5	4	3	2	1	0
ss_manual_mode	ss_rdm_ctrl[2:0]			ss_tri_ctrl[3:0]			
R/W	R/W			R/W			

Bit	Field	Type	Reset	Description
7	ss_manual_mode	R/W	0	0: disable 1: enable
[6:4]	ss_rdm_ctrl[2:0]	R/W	000	000: no dither 001: 1 bit 010: 2 bits 011: 3 bits 100: 4 bits 101: no dither 110: 0.5 bit
[3:0]	ss_tri_ctrl[3:0]	R/W	0000	ss range is changed based on ramp clk option

9.2.2.6 DIG_SS_CTRL3_LEVEL1 (Page 1,Offset=2Dh) [Reset=0x80]

7	6	5	4	3	2	1	0
ramp_tm_freq_ctrl[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
[7:0]	ramp_tm_freq_ctrl[7:0]	R/W	10000000	

9.2.2.7 DIG_SS_CTRL4_LEVEL1 (Page 1,Offset=2Eh) [Reset=0xC4]

7	6	5	4	3	2	1	0
ss_tm_dstep_ctrl[3:0]				ss_tm_ustep_ctrl[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
[7:4]	ss_tm_dstep_ctrl[3:0]	R/W	1100	
[3:0]	ss_tm_ustep_ctrl[3:0]	R/W	0100	

9.2.2.8 DIG_SS_CTRL5_LEVEL1 (Page 1,Offset=2Fh) [Reset=0x58]

7	6	5	4	3	2	1	0
ramp_tm_amp_ctrl[1:0]			ss_tm_period_boundry[5:0]				
R/W			R/W				

Bit	Field	Type	Reset	Description
[7:6]	ramp_tm_amp_ctrl[1:0]	R/W	01	
[5:0]	ss_tm_period_boundry[5:0]	R/W	011000	

9.2.2.9 DIG_AC_DIAG_FULL_RPT1 (Page 1,Offset=37h) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_high_ch1_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_high_ch1_full[7:0]	R/W	00000000	CH1 [23:16] of ac_amp det_raw data

9.2.2.10 DIG_AC_DIAG_FULL_RPT2 (Page 1,Offset=38h) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_mid_ch1_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_mid_ch1_full[7:0]	R/W	00000000	CH1 [15:8] of ac_amp det_raw data

9.2.2.11 DIG_AC_DIAG_FULL_RPT3 (Page 1,Offset=39h) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_low_ch1_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_low_ch1_full[7:0]	R/W	00000000	CH1 [7:0] of ac_amp det_raw data

9.2.2.12 DIG_AC_DIAG_FULL_RPT4 (Page 1,Offset=3Ah) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_high_ch2_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_high_ch2_full[7:0]	R/W	00000000	CH2 [23:16] of ac_amp det_raw data

9.2.2.13 DIG_AC_DIAG_FULL_RPT5 (Page 1,Offset=3Bh) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_mid_ch2_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_mid_ch2_full[7:0]	R/W	00000000	CH2 [15:8] of ac_amp det_raw data

9.2.2.14 DIG_AC_DIAG_FULL_RPT6 (Page 1,Offset=3Ch) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_low_ch2_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_low_ch2_full[7:0]	R/W	00000000	CH2 [7:0] of ac_amp det_raw data

9.2.2.15 DIG_AC_DIAG_FULL_RPT7 (Page 1,Offset=3Dh) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_amp_high_ch3_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_high_ch3_full[7:0]	R/W	00000000	CH3 [23:16] of ac_amp det_raw data

9.2.2.16 DIG_AC_DIAG_FULL_RPT8 (Page 1,Offset=3Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_amp_mid_ch3_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_mid_ch3_full[7:0]	R/W	00000000	CH3 [15:8] of ac_amp det_raw data

9.2.2.17 DIG_AC_DIAG_FULL_RPT9 (Page 1, Offset=3Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_amp_low_ch3_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_low_ch3_full[7:0]	R/W	00000000	CH3 [7:0] of ac_amp det_raw data

9.2.2.18 DIG_AC_DIAG_FULL_RPT10 (Page 1, Offset=40h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_amp_high_ch4_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_high_ch4_full[7:0]	R/W	00000000	CH4 [23:16] of ac_amp det_raw data

9.2.2.19 DIG_AC_DIAG_FULL_RPT11 (Page 1, Offset=41h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_amp_mid_ch4_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_mid_ch4_full[7:0]	R/W	00000000	CH4 [15:8] of ac_amp det_raw data

9.2.2.20 DIG_AC_DIAG_FULL_RPT12 (Page 1, Offset=42h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_amp_low_ch4_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_amp_low_ch4_full[7:0]	R/W	00000000	CH4 [7:0] of ac_amp det_raw data

9.2.2.21 DIG_AC_DIAG_FULL_RPT13 (Page 1, Offset=43h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_phase_high_ch1_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_high_ch1_full[7:0]	R/W	00000000	CH1 [23:16] of ac_phase raw data

9.2.2.22 DIG_AC_DIAG_FULL_RPT14 (Page 1,Offset=44h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_phase_mid_ch1_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_mid_ch1_full[7:0]	R/W	00000000	CH1 [15:8] of ac_phase raw data

9.2.2.23 DIG_AC_DIAG_FULL_RPT15 (Page 1,Offset=45h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_phase_low_ch1_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_low_ch1_full[7:0]	R/W	00000000	CH1 [7:0] of ac_phase raw data

9.2.2.24 DIG_AC_DIAG_FULL_RPT16 (Page 1,Offset=46h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_phase_high_ch2_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_high_ch2_full[7:0]	R/W	00000000	CH2 [23:16] of ac_phase raw data

9.2.2.25 DIG_AC_DIAG_FULL_RPT17 (Page 1,Offset=47h) [Reset=0x00]

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

ac_phase_mid_ch2_full[7:0]

RO

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_mid_ch2_full[7:0]	R/W	00000000	CH2 [15:8] of ac_phase raw data

9.2.2.26 DIG_AC_DIAG_FULL_RPT18 (Page 1, Offset=48h) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_low_ch2_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_low_ch2_full[7:0]	R/W	00000000	CH2 [7:0] of ac_phase raw data

9.2.2.27 DIG_AC_DIAG_FULL_RPT19 (Page 1, Offset=49h) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_high_ch3_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
[7:0]	ac_phase_high_ch3_full[7:0]	R/W	00000000	CH3 [23:16] of ac_phase raw data

9.2.2.28 DIG_AC_DIAG_FULL_RPT20 (Page 1, Offset=4Ah) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_mid_ch3_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	ac_phase_mid_ch3_full[7:0]	R/W	00000000	CH3 [15:8] of ac_phase raw data

9.2.2.29 DIG_AC_DIAG_FULL_RPT21 (Page 1, Offset=4Bh) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_low_ch3_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	ac_phase_low_ch3_full[7:0]	R/W	00000000	CH3 [7:0] of ac_phase raw data

9.2.2.30 DIG_AC_DIAG_FULL_RPT22 (Page 1, Offset=4Ch) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_high_ch4_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	ac_phase_high_ch4_full[7:0]	R/W	00000000	CH4 [23:16] of ac_phase raw data

9.2.2.31 DIG_AC_DIAG_FULL_RPT23 (Page 1,Offset=4Dh) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_mid_ch4_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	ac_phase_mid_ch4_full[7:0]	R/W	00000000	CH4 [15:8] of ac_phase raw data

9.2.2.32 DIG_AC_DIAG_FULL_RPT24 (Page 1,Offset=4Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
ac_phase_low_ch4_full[7:0]							
RO							

Bit	Field	Type	Reset	Description
7:0	ac_phase_low_ch4_full[7:0]	R/W	00000000	CH4 [7:0] of ac_phase raw data

9.2.2.33 DIG_SDOUT_PAD_CTRL (Page 1,Offset=50h) [Reset=0x29]

7	6	5	4	3	2	1	0
Reserved		sdout_oe	Sdout_sel				
R/W		R/W	R/W				

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	00	This bit is reserved
5	sdout_oe	R/W	1	0: SDOUT pin is input 1: Config SDOUT_PAD to be output
[4:0]	Sdout_sel	R/W	01001	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO1 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.34 DIG_GPIO0_PAD_CTRL (Page 1,Offset=51h) [Reset=0x28]

7	6	5	4	3	2	1	0
Reserved		gpio0_oe	gpio0_sel[4:0]				

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	00	
5	gpio0_oe	R/W	1	0: gpio0 pin is input 1: Config GPIO0_PAD to be output
[4:0]	gpio0_sel[4:0]	R/W	01000	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO1 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.35 DIG_GPIO1_PAD_CTRL (Page 1,Offset=52h) [Reset=0x00]

7	6	5	4	3	2	1	0
Reserved		GPIO1_oe	GPIO1_sel[4:0]				
R/W		R/W	R/W				

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	00	
5	GPIO1_oe	R/W	0	0: GPIO1 pin is input 1: Config GPIO1_PAD to be output
[4:0]	GPIO1_sel[4:0]	R/W	00000	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO1 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.36 DIG_GPIO2_PAD_CTRL (Page 1,Offset=53h) [Reset=0x00]

7	6	5	4	3	2	1	0

Reserved	Gpio2_oe	Gpio2_sel[4:0]
R/W	R/W	R/W

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	0	
5	Gpio2_oe	R/W	0	0: GPIO2 pin is input 1: Config GPIO2_PAD to be output
[4:0]	Gpio2_sel[4:0]	R/W	0	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio2 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO2 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.37 DIG_GPIO3_PAD_CTRL (Page 1,Offset=54h) [Reset=0x2B]

7	6	5	4	3	2	1	0
Reserved		Gpio3_oe	Gpio3_sel[4:0]				
R/W		R/W	R/W				

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	00	
5	Gpio3_oe	R/W	1	0: GPIO3 pin is input 1: Config GPIO3_PAD to be output
[4:0]	Gpio3_sel[4:0]	R/W	01011	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio3 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO3 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.38 DIG_GPIO4_PAD_CTRL (Page 1, Offset=55h) [Reset=0x05]

7	6	5	4	3	2	1	0
Reserved		Gpio3_oe	Gpio3_sel[4:0]				
R/W		R/W	R/W				

Bit	Field	Type	Reset	Description
[7:6]	reserved	R/W	00	
5	Gpio3_oe	R/W	0	0: GPIO3 pin is input 1: Config GPIO3_PAD to be output
[4:0]	Gpio3_sel[4:0]	R/W	00101	0000: off(low) 0001: deep sleep 0010: sleep 0011: hiz 0100: ramp_sync_gpio 0101: mute 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: gpio3 as WARNZ output 1001: serial audio interface data output(SDOUT) 1010: serial audio interface data output(SDOUT2) 1011: GPIO3 as FAULTZ output 1100: resetz *internal* 10000: PLL clock/8 10001: osc clock /4 10010: clock error flag 10011: clock halt detection flag 10100: reserved 10110: DSP boot done flag others: N/A(zero)

9.2.2.39 DIG_VBAT_OVUV_SEL1 (Page 1, Offset=56h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_vbat_ov_sel	gpio2_vbat_uv_sel	gpio1_vbat_ov_sel	gpio1_vbat_uv_sel	gpio0_vbat_ov_sel	gpio0_vbat_uv_sel	sdout_vbat_ov_sel	sdout_vbat_uv_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on GPIO2 1: Un-mask VBAT over voltage fault on GPIO2
6	gpio2_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on GPIO2 1: Un-mask VBAT under voltage fault on GPIO2
5	gpio1_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on GPIO1 1: Un-mask VBAT over voltage fault on GPIO1
4	gpio1_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on GPIO1 1: Un-mask VBAT under voltage fault on GPIO1
3	gpio0_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on GPIO0 1: Un-mask VBAT over voltage fault on GPIO0
2	gpio0_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on GPIO0 1: Un-mask VBAT under voltage fault on GPIO0
1	sdout_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on SDOUT 1: Un-mask VBAT over voltage fault on SDOUT
0	sdout_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on SDOUT 1: Un-mask VBAT under voltage fault on SDOUT

9.2.2.40 DIG_VBAT_OVUV_SEL2 (Page 1, Offset=57h) [Reset=0xFF]

7	6	5	4	3	2	1	0
Reserved				gpio4_vbat_ov_sel	gpio4_vbat_uv_sel	gpio3_vbat_ov_sel	gpio3_vbat_uv_sel
R/W				R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
[7:4]	Reserved	R/W	1111	Reserved
3	gpio4_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on GPIO4 1: Un-mask VBAT over voltage fault on GPIO4
2	gpio4_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on GPIO4 1: Un-mask VBAT under voltage fault on GPIO4
1	gpio3_vbat_ov_sel	R/W	1	0: Mask VBAT over voltage fault on GPIO3 1: Un-mask VBAT over voltage fault on GPIO3
0	gpio3_vbat_uv_sel	R/W	1	0: Mask VBAT under voltage fault on GPIO3 1: Un-mask VBAT under voltage fault on GPIO3

9.2.2.41 DIG_FAULT_SDOU_SEL1 (Page 1,Offset=58h) [Reset=0xFF]

7	6	5	4	3	2	1	0
sdout_clk_fault_sel	sdout_pvdd_uv_sel	sdout_pvdd_ov_sel	sdout_otsd_global_sel	sdout_otsd_ch4_sel	sdout_otsd_ch3_sel	sdout_otsd_ch2_sel	sdout_otsd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	sdout_clk_fault_sel	R/W	1	0: Mask clock fault report on SDOU 1: Un-mask clock fault report on SDOU
6	sdout_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on SDOU 1: Un-mask PVDD under voltage fault report on SDOU
5	sdout_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on SDOU 1: Un-mask PVDD over voltage fault report on SDOU
4	sdout_otsd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on SDOU 1: Un-mask global over temperature shutdown fault report on SDOU
3	sdout_otsd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on SDOU 1: Un-mask CH4 over temperature shutdown fault report on SDOU
2	sdout_otsd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on SDOU 1: Un-mask CH3 over temperature shutdown fault report on SDOU
1	sdout_otsd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on SDOU 1: Un-mask CH2 over temperature shutdown fault report on SDOU
0	sdout_otsd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on SDOU 1: Un-mask CH1 over temperature shutdown fault report on SDOU

9.2.2.42 DIG_FAULT_SDOU_SEL2 (Page 1,Offset=59h) [Reset=0xFF]

7	6	5	4	3	2	1	0
sdout_dc_ch4_sel	sdout_dc_ch3_sel	sdout_dc_ch2_sel	sdout_dc_ch1_sel	sdout_oc_ch4_sel	sdout_oc_ch3_sel	sdout_oc_ch2_sel	sdout_oc_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	sdout_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on SDOU 1: Un-mask CH4 dc fault report on SDOU
6	sdout_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on SDOU 1: Un-mask CH3 dc fault report on SDOU
5	sdout_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on SDOU 1: Un-mask CH2 dc fault report on SDOU
4	sdout_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on SDOU 1: Un-mask CH1 dc fault report on SDOU
3	sdout_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on SDOU 1: Un-mask CH4 over current fault report on SDOU
2	sdout_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on SDOU 1: Un-mask CH3 over current fault report on SDOU
1	sdout_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on SDOU 1: Un-mask CH2 over current fault report on SDOU
0	sdout_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on SDOU 1: Un-mask CH1 over current fault report on SDOU

9.2.2.43 DIG_FAULT_SDOUT_SEL3 (Page 1,Offset=5Ah) [Reset=0xFF]

7	6	5	4	3	2	1	0
sdout_clip_ch4_sel	sdout_clip_ch3_sel	sdout_clip_ch2_sel	sdout_clip_ch1_sel	sdout_otw_ch4_sel	sdout_otw_ch3_sel	sdout_otw_ch2_sel	sdout_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	sdout_clip_ch4_sel	R/W	1	0: Mask CH4 clip on SDOUT 1: Un-mask CH4 dc fault report on SDOUT
6	sdout_clip_ch3_sel	R/W	1	0: Mask CH3 clip on SDOUT 1: Un-mask CH3 dc fault report on SDOUT
5	sdout_clip_ch2_sel	R/W	1	0: Mask CH2 clip on SDOUT 1: Un-mask CH2 dc fault report on SDOUT
4	sdout_clip_ch1_sel	R/W	1	0: Mask CH1 clip on SDOUT 1: Un-mask CH1 dc fault report on SDOUT
3	sdout_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on SDOUT 1: Un-mask CH4 OT warning report on SDOUT
2	sdout_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on SDOUT 1: Un-mask CH3 OT warning report on SDOUT
1	sdout_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on SDOUT 1: Un-mask CH2 OT warning report on SDOUT
0	sdout_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on SDOUT 1: Un-mask CH1 OT warning report on SDOUT

9.2.2.44 DIG_FAULT_SDOUT_SEL4 (Page 1,Offset=5Bh) [Reset=0xFF]

7	6	5	4	3	2	1	0
sdout_cbc_warn_ch4_sel	sdout_cbc_warn_ch3_sel	sdout_cbc_warn_ch2_sel	sdout_cbc_warn_ch1_sel	sdout_cbc_fault_ch4_sel	sdout_cbc_fault_ch3_sel	sdout_cbc_fault_ch2_sel	sdout_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	sdout_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on SDOUT 1: Un-mask CH4 CBC warning report on SDOUT
6	sdout_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on SDOUT 1: Un-mask CH3 CBC warning report on SDOUT
5	sdout_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on SDOUT 1: Un-mask CH2 CBC warning report on SDOUT
4	sdout_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on SDOUT 1: Un-mask CH1 CBC warning report on SDOUT
3	sdout_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on SDOUT 1: Un-mask CH4 CBC fault report on SDOUT
2	sdout_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on SDOUT 1: Un-mask CH3 CBC fault report on SDOUT
1	sdout_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on SDOUT 1: Un-mask CH2 CBC fault report on SDOUT
0	sdout_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on SDOUT 1: Un-mask CH1 CBC fault report on SDOUT

9.2.2.45 DIG_FAULT_SDOUT_SEL5 (Page 1,Offset=5Ch) [Reset=0xFF]

7	6	5	4	3	2	1	0
sdout_rtlldg_ol_det_ch4_sel	sdout_rtlldg_ol_det_ch3_sel	sdout_rtlldg_ol_det_ch2_sel	sdout_rtlldg_ol_det_ch1_sel	sdout_rtlldg_sl_det_ch4_sel	sdout_rtlldg_sl_det_ch3_sel	sdout_rtlldg_sl_det_ch2_sel	sdout_rtlldg_sl_det_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	sdout_rtlldg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on SDOUT 1: Un-mask CH4 real-time open load on SDOUT
6	sdout_rtlldg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on SDOUT 1: Un-mask CH3 real-time open load on SDOUT

Bit	Field	Type	Reset	Description
5	sdout_rtlldg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on SDOUT 1: Un-mask CH2 real-time open load on SDOUT
4	sdout_rtlldg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on SDOUT 1: Un-mask CH1 real-time open load on SDOUT
3	sdout_rtlldg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on SDOUT 1: Un-mask CH4 real-time short load on SDOUT
2	sdout_rtlldg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on SDOUT 1: Un-mask CH3 real-time short load on SDOUT
1	sdout_rtlldg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on SDOUT 1: Un-mask CH2 real-time short load on SDOUT
0	sdout_rtlldg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on SDOUT 1: Un-mask CH1 real-time short load on SDOUT

9.2.2.46 DIG_FAULT_GPIO0_SEL1 (Page 1,Offset=5Dh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio0_clk_fault_sel	gpio0_pvdd_uv_sel	gpio0_pvdd_ov_sel	gpio0_otsd_global_sel	gpio0_otsd_ch4_sel	gpio0_otsd_ch3_sel	gpio0_otsd_ch2_sel	gpio0_otsd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio0_clk_fault_sel	R/W	1	0: Mask clock fault report on GPIO0 1: Un-mask clock fault report on GPIO0
6	gpio0_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on GPIO0 1: Un-mask PVDD under voltage fault report on GPIO0
5	gpio0_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on GPIO0 1: Un-mask PVDD over voltage fault report on GPIO0
4	gpio0_otsd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on GPIO0 1: Un-mask global over temperature shutdown fault report on GPIO0
3	gpio0_otsd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on GPIO0 1: Un-mask CH4 over temperature shutdown fault report on GPIO0
2	gpio0_otsd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on GPIO0 1: Un-mask CH3 over temperature shutdown fault report on GPIO0
1	gpio0_otsd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on GPIO0 1: Un-mask CH2 over temperature shutdown fault report on GPIO0
0	gpio0_otsd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on GPIO0 1: Un-mask CH1 over temperature shutdown fault report on GPIO0

9.2.2.47 DIG_FAULT_GPIO0_SEL2 (Page 1,Offset=5Eh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio0_dc_ch4_sel	gpio0_dc_ch3_sel	gpio0_dc_ch2_sel	gpio0_dc_ch1_sel	gpio0_oc_ch4_sel	gpio0_oc_ch3_sel	gpio0_oc_ch2_sel	gpio0_oc_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio0_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on GPIO0 1: Un-mask CH4 dc fault report on GPIO0
6	gpio0_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on GPIO0 1: Un-mask CH3 dc fault report on GPIO0
5	gpio0_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on GPIO0 1: Un-mask CH2 dc fault report on GPIO0
4	gpio0_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on GPIO0 1: Un-mask CH1 dc fault report on GPIO0
3	gpio0_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on GPIO0 1: Un-mask CH4 over current fault report on GPIO0
2	gpio0_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on GPIO0 1: Un-mask CH3 over current fault report on GPIO0
1	gpio0_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on GPIO0 1: Un-mask CH2 over current fault report on GPIO0

Bit	Field	Type	Reset	Description
0	gpio0_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on GPIO0 1: Un-mask CH1 over current fault report on GPIO0

9.2.2.48 DIG_FAULT_GPIO0_SEL3 (Page 1, Offset=5Fh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio0_clip_ch4_sel	gpio0_clip_ch3_sel	gpio0_clip_ch2_sel	gpio0_clip_ch1_sel	gpio0_otw_ch4_sel	gpio0_otw_ch3_sel	gpio0_otw_ch2_sel	gpio0_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio0_clip_ch4_sel	R/W	1	0: Mask CH4 clip on GPIO0 1: Un-mask CH4 dc fault report on GPIO0
6	gpio0_clip_ch3_sel	R/W	1	0: Mask CH3 clip on GPIO0 1: Un-mask CH3 dc fault report on GPIO0
5	gpio0_clip_ch2_sel	R/W	1	0: Mask CH2 clip on GPIO0 1: Un-mask CH2 dc fault report on GPIO0
4	gpio0_clip_ch1_sel	R/W	1	0: Mask CH1 clip on GPIO0 1: Un-mask CH1 dc fault report on GPIO0
3	gpio0_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on GPIO0 1: Un-mask CH4 OT warning report on GPIO0
2	gpio0_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on GPIO0 1: Un-mask CH3 OT warning report on GPIO0
1	gpio0_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on GPIO0 1: Un-mask CH2 OT warning report on GPIO0
0	gpio0_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on GPIO0 1: Un-mask CH1 OT warning report on GPIO0

9.2.2.49 DIG_FAULT_GPIO0_SEL4 (Page 1, Offset=60h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio0_cbc_warn_ch4_sel	gpio0_cbc_warn_ch3_sel	gpio0_cbc_warn_ch2_sel	gpio0_cbc_warn_ch1_sel	gpio0_cbc_fault_ch4_sel	gpio0_cbc_fault_ch3_sel	gpio0_cbc_fault_ch2_sel	gpio0_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio0_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on GPIO0 1: Un-mask CH4 CBC warning report on GPIO0
6	gpio0_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on GPIO0 1: Un-mask CH3 CBC warning report on GPIO0
5	gpio0_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on GPIO0 1: Un-mask CH2 CBC warning report on GPIO0
4	gpio0_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on GPIO0 1: Un-mask CH1 CBC warning report on GPIO0
3	gpio0_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on GPIO0 1: Un-mask CH4 CBC fault report on GPIO0
2	gpio0_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on GPIO0 1: Un-mask CH3 CBC fault report on GPIO0
1	gpio0_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on GPIO0 1: Un-mask CH2 CBC fault report on GPIO0
0	gpio0_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on GPIO0 1: Un-mask CH1 CBC fault report on GPIO0

9.2.2.50 DIG_FAULT_GPIO0_SEL5 (Page 1, Offset=61h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio0_rtdg_sl_det_ch4_sel	gpio0_rtdg_sl_det_ch3_sel	gpio0_rtdg_sl_det_ch2_sel	gpio0_rtdg_sl_det_ch1_sel	gpio0_rtdg_sl_det_ch4_sel	gpio0_rtdg_sl_det_ch3_sel	gpio0_rtdg_sl_det_ch2_sel	gpio0_rtdg_sl_det_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio0_rtl_dg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on GPIO0 1: Un-mask CH4 real-time open load on GPIO0
6	gpio0_rtl_dg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on GPIO0 1: Un-mask CH3 real-time open load on GPIO0
5	gpio0_rtl_dg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on GPIO0 1: Un-mask CH2 real-time open load on GPIO0
4	gpio0_rtl_dg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on GPIO0 1: Un-mask CH1 real-time open load on GPIO0
3	gpio0_rtl_dg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on GPIO0 1: Un-mask CH4 real-time short load on GPIO0
2	gpio0_rtl_dg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on GPIO0 1: Un-mask CH3 real-time short load on GPIO0
1	gpio0_rtl_dg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on GPIO0 1: Un-mask CH2 real-time short load on GPIO0
0	gpio0_rtl_dg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on GPIO0 1: Un-mask CH1 real-time short load on GPIO0

9.2.2.51 DIG_FAULT_GPIO1_SEL1 (Page 1, Offset=62h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio1_clk_fault_sel	gpio1_pvdd_uv_sel	gpio1_pvdd_ov_sel	gpio1_otsd_global_sel	gpio1_otsd_ch4_sel	gpio1_otsd_ch3_sel	gpio1_otsd_ch2_sel	gpio1_otsd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio1_clk_fault_sel	R/W	1	0: Mask clock fault report on GPIO1 1: Un-mask clock fault report on GPIO1
6	gpio1_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on GPIO1 1: Un-mask PVDD under voltage fault report on GPIO1
5	gpio1_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on GPIO1 1: Un-mask PVDD over voltage fault report on GPIO1
4	gpio1_otsd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on GPIO1 1: Un-mask global over temperature shutdown fault report on GPIO1
3	gpio1_otsd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on GPIO1 1: Un-mask CH4 over temperature shutdown fault report on GPIO1
2	gpio1_otsd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on GPIO1 1: Un-mask CH3 over temperature shutdown fault report on GPIO1
1	gpio1_otsd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on GPIO1 1: Un-mask CH2 over temperature shutdown fault report on GPIO1
0	gpio1_otsd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on GPIO1 1: Un-mask CH1 over temperature shutdown fault report on GPIO1

9.2.2.52 DIG_FAULT_GPIO1_SEL2 (Page 1, Offset=63h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio1_dc_ch4_sel	gpio1_dc_ch3_sel	gpio1_dc_ch2_sel	gpio1_dc_ch1_sel	gpio1_oc_ch4_sel	gpio1_oc_ch3_sel	gpio1_oc_ch2_sel	gpio1_oc_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio1_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on GPIO1 1: Un-mask CH4 dc fault report on GPIO1
6	gpio1_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on GPIO1 1: Un-mask CH3 dc fault report on GPIO1
5	gpio1_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on GPIO1 1: Un-mask CH2 dc fault report on GPIO1
4	gpio1_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on GPIO1 1: Un-mask CH1 dc fault report on GPIO1
3	gpio1_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on GPIO1 1: Un-mask CH4 over current fault report on GPIO1

Bit	Field	Type	Reset	Description
2	gpio1_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on GPIO1 1: Un-mask CH3 over current fault report on GPIO1
1	gpio1_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on GPIO1 1: Un-mask CH2 over current fault report on GPIO1
0	gpio1_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on GPIO1 1: Un-mask CH1 over current fault report on GPIO1

9.2.2.53 DIG_FAULT_GPIO1_SEL3 (Page 1,Offset=64h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio1_clip_ch4_sel	gpio1_clip_ch3_sel	gpio1_clip_ch2_sel	gpio1_clip_ch1_sel	gpio1_otw_ch4_sel	gpio1_otw_ch3_sel	gpio1_otw_ch2_sel	gpio1_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio1_clip_ch4_sel	R/W	1	0: Mask CH4 clip on GPIO1 1: Un-mask CH4 dc fault report on GPIO1
6	gpio1_clip_ch3_sel	R/W	1	0: Mask CH3 clip on GPIO1 1: Un-mask CH3 dc fault report on GPIO1
5	gpio1_clip_ch2_sel	R/W	1	0: Mask CH2 clip on GPIO1 1: Un-mask CH2 dc fault report on GPIO1
4	gpio1_clip_ch1_sel	R/W	1	0: Mask CH1 clip on GPIO1 1: Un-mask CH1 dc fault report on GPIO1
3	gpio1_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on GPIO1 1: Un-mask CH4 OT warning report on GPIO1
2	gpio1_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on GPIO1 1: Un-mask CH3 OT warning report on GPIO1
1	gpio1_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on GPIO1 1: Un-mask CH2 OT warning report on GPIO1
0	gpio1_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on GPIO1 1: Un-mask CH1 OT warning report on GPIO1

9.2.2.54 DIG_FAULT_GPIO1_SEL4 (Page 1,Offset=65h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio1_cbc_warn_ch4_sel	gpio1_cbc_warn_ch3_sel	gpio1_cbc_warn_ch2_sel	gpio1_cbc_warn_ch1_sel	gpio1_cbc_fault_ch4_sel	gpio1_cbc_fault_ch3_sel	gpio1_cbc_fault_ch2_sel	gpio1_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio1_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on GPIO1 1: Un-mask CH4 CBC warning report on GPIO1
6	gpio1_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on GPIO1 1: Un-mask CH3 CBC warning report on GPIO1
5	gpio1_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on GPIO1 1: Un-mask CH2 CBC warning report on GPIO1
4	gpio1_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on GPIO1 1: Un-mask CH1 CBC warning report on GPIO1
3	gpio1_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on GPIO1 1: Un-mask CH4 CBC fault report on GPIO1
2	gpio1_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on GPIO1 1: Un-mask CH3 CBC fault report on GPIO1
1	gpio1_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on GPIO1 1: Un-mask CH2 CBC fault report on GPIO1
0	gpio1_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on GPIO1 1: Un-mask CH1 CBC fault report on GPIO1

9.2.2.55 DIG_FAULT_GPIO1_SEL5 (Page 1,Offset=66h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio1_rtdg_sl_det_ch4_sel	gpio1_rtdg_sl_det_ch3_sel	gpio1_rtdg_sl_det_ch2_sel	gpio1_rtdg_sl_det_ch1_sel	gpio1_rtdg_sl_det_ch4_sel	gpio1_rtdg_sl_det_ch3_sel	gpio1_rtdg_sl_det_ch2_sel	gpio1_rtdg_sl_det_ch1_sel

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
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Bit	Field	Type	Reset	Description
7	gpio1_rtl_dg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on GPIO1 1: Un-mask CH4 real-time open load on GPIO1
6	gpio1_rtl_dg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on GPIO1 1: Un-mask CH3 real-time open load on GPIO1
5	gpio1_rtl_dg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on GPIO1 1: Un-mask CH2 real-time open load on GPIO1
4	gpio1_rtl_dg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on GPIO1 1: Un-mask CH1 real-time open load on GPIO1
3	gpio1_rtl_dg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on GPIO1 1: Un-mask CH4 real-time short load on GPIO1
2	gpio1_rtl_dg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on GPIO1 1: Un-mask CH3 real-time short load on GPIO1
1	gpio1_rtl_dg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on GPIO1 1: Un-mask CH2 real-time short load on GPIO1
0	gpio1_rtl_dg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on GPIO1 1: Un-mask CH1 real-time short load on GPIO1

9.2.2.56 DIG_FAULT_GPIO2_SEL1 (Page 1, Offset=67h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_clk_fault_sel	gpio2_pvdd_uv_sel	gpio2_pvdd_ov_sel	gpio2_otsd_global_sel	gpio2_otsd_ch4_sel	gpio2_otsd_ch3_sel	gpio2_otsd_ch2_sel	gpio2_otsd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_clk_fault_sel	R/W	1	0: Mask clock fault report on GPIO2 1: Un-mask clock fault report on GPIO2
6	gpio2_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on GPIO2 1: Un-mask PVDD under voltage fault report on GPIO2
5	gpio2_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on GPIO2 1: Un-mask PVDD over voltage fault report on GPIO2
4	gpio2_otsd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on GPIO2 1: Un-mask global over temperature shutdown fault report on GPIO2
3	gpio2_otsd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on GPIO2 1: Un-mask CH4 over temperature shutdown fault report on GPIO2
2	gpio2_otsd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on GPIO2 1: Un-mask CH3 over temperature shutdown fault report on GPIO2
1	gpio2_otsd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on GPIO2 1: Un-mask CH2 over temperature shutdown fault report on GPIO2
0	gpio2_otsd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on GPIO2 1: Un-mask CH1 over temperature shutdown fault report on GPIO2

9.2.2.57 DIG_FAULT_GPIO2_SEL2 (Page 1, Offset=68h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_dc_ch4_sel	gpio2_dc_ch3_sel	gpio2_dc_ch2_sel	gpio2_dc_ch1_sel	gpio2_oc_ch4_sel	gpio2_oc_ch3_sel	gpio2_oc_ch2_sel	gpio2_oc_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on GPIO2 1: Un-mask CH4 dc fault report on GPIO2
6	gpio2_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on GPIO2 1: Un-mask CH3 dc fault report on GPIO2
5	gpio2_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on GPIO2 1: Un-mask CH2 dc fault report on GPIO2

Bit	Field	Type	Reset	Description
4	gpio2_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on GPIO2 1: Un-mask CH1 dc fault report on GPIO2
3	gpio2_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on GPIO2 1: Un-mask CH4 over current fault report on GPIO2
2	gpio2_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on GPIO2 1: Un-mask CH3 over current fault report on GPIO2
1	gpio2_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on GPIO2 1: Un-mask CH2 over current fault report on GPIO2
0	gpio2_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on GPIO2 1: Un-mask CH1 over current fault report on GPIO2

9.2.2.58 DIG_FAULT_GPIO2_SEL3 (Page 1, Offset=69h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_clip_ch4_sel	gpio2_clip_ch3_sel	gpio2_clip_ch2_sel	gpio2_clip_ch1_sel	gpio2_otw_ch4_sel	gpio2_otw_ch3_sel	gpio2_otw_ch2_sel	gpio2_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_clip_ch4_sel	R/W	1	0: Mask CH4 clip on GPIO2 1: Un-mask CH4 dc fault report on GPIO2
6	gpio2_clip_ch3_sel	R/W	1	0: Mask CH3 clip on GPIO2 1: Un-mask CH3 dc fault report on GPIO2
5	gpio2_clip_ch2_sel	R/W	1	0: Mask CH2 clip on GPIO2 1: Un-mask CH2 dc fault report on GPIO2
4	gpio2_clip_ch1_sel	R/W	1	0: Mask CH1 clip on GPIO2 1: Un-mask CH1 dc fault report on GPIO2
3	gpio2_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on GPIO2 1: Un-mask CH4 OT warning report on GPIO2
2	gpio2_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on GPIO2 1: Un-mask CH3 OT warning report on GPIO2
1	gpio2_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on GPIO2 1: Un-mask CH2 OT warning report on GPIO2
0	gpio2_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on GPIO2 1: Un-mask CH1 OT warning report on GPIO2

9.2.2.59 DIG_FAULT_GPIO2_SEL4 (Page 1, Offset=6Ah) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_cbc_warn_ch4_sel	gpio2_cbc_warn_ch3_sel	gpio2_cbc_warn_ch2_sel	gpio2_cbc_warn_ch1_sel	gpio2_cbc_fault_ch4_sel	gpio2_cbc_fault_ch3_sel	gpio2_cbc_fault_ch2_sel	gpio2_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on GPIO2 1: Un-mask CH4 CBC warning report on GPIO2
6	gpio2_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on GPIO2 1: Un-mask CH3 CBC warning report on GPIO2
5	gpio2_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on GPIO2 1: Un-mask CH2 CBC warning report on GPIO2
4	gpio2_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on GPIO2 1: Un-mask CH1 CBC warning report on GPIO2
3	gpio2_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on GPIO2 1: Un-mask CH4 CBC fault report on GPIO2
2	gpio2_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on GPIO2 1: Un-mask CH3 CBC fault report on GPIO2
1	gpio2_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on GPIO2 1: Un-mask CH2 CBC fault report on GPIO2
0	gpio2_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on GPIO2 1: Un-mask CH1 CBC fault report on GPIO2

9.2.2.60 DIG_FAULT_GPIO2_SEL5 (Page 1,Offset=6Bh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio2_rtdg_ol_det_ch4_sel	gpio2_rtdg_ol_det_ch3_sel	gpio2_rtdg_ol_det_ch2_sel	gpio2_rtdg_ol_det_ch1_sel	gpio2_rtdg_sl_det_ch4_sel	gpio2_rtdg_sl_det_ch3_sel	gpio2_rtdg_sl_det_ch2_sel	gpio2_rtdg_sl_det_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio2_rtdg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on GPIO2 1: Un-mask CH4 real-time open load on GPIO2
6	gpio2_rtdg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on GPIO2 1: Un-mask CH3 real-time open load on GPIO2
5	gpio2_rtdg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on GPIO2 1: Un-mask CH2 real-time open load on GPIO2
4	gpio2_rtdg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on GPIO2 1: Un-mask CH1 real-time open load on GPIO2
3	gpio2_rtdg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on GPIO2 1: Un-mask CH4 real-time short load on GPIO2
2	gpio2_rtdg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on GPIO2 1: Un-mask CH3 real-time short load on GPIO2
1	gpio2_rtdg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on GPIO2 1: Un-mask CH2 real-time short load on GPIO2
0	gpio2_rtdg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on GPIO2 1: Un-mask CH1 real-time short load on GPIO2

9.2.2.61 DIG_FAULT_GPIO3_SEL1 (Page 1,Offset=6Ch) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio3_clk_fault_sel	gpio3_pvdd_uv_sel	gpio3_pvdd_ov_sel	gpio3_otstd_global_sel	gpio3_otstd_ch4_sel	gpio3_otstd_ch3_sel	gpio3_otstd_ch2_sel	gpio3_otstd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio3_clk_fault_sel	R/W	1	0: Mask clock fault report on GPIO3 1: Un-mask clock fault report on GPIO3
6	gpio3_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on GPIO3 1: Un-mask PVDD under voltage fault report on GPIO3
5	gpio3_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on GPIO3 1: Un-mask PVDD over voltage fault report on GPIO3
4	gpio3_otstd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on GPIO3 1: Un-mask global over temperature shutdown fault report on GPIO3
3	gpio3_otstd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on GPIO3 1: Un-mask CH4 over temperature shutdown fault report on GPIO3
2	gpio3_otstd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on GPIO3 1: Un-mask CH3 over temperature shutdown fault report on GPIO3
1	gpio3_otstd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on GPIO3 1: Un-mask CH2 over temperature shutdown fault report on GPIO3
0	gpio3_otstd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on GPIO3 1: Un-mask CH1 over temperature shutdown fault report on GPIO3

9.2.2.62 DIG_FAULT_GPIO3_SEL2 (Page 1,Offset=6Dh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio3_dc_ch4_sel	gpio3_dc_ch3_sel	gpio3_dc_ch2_sel	gpio3_dc_ch1_sel	gpio3_oc_ch4_sel	gpio3_oc_ch3_sel	gpio3_oc_ch2_sel	gpio3_oc_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio3_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on GPIO3 1: Un-mask CH4 dc fault report on GPIO3
6	gpio3_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on GPIO3 1: Un-mask CH3 dc fault report on GPIO3
5	gpio3_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on GPIO3 1: Un-mask CH2 dc fault report on GPIO3
4	gpio3_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on GPIO3 1: Un-mask CH1 dc fault report on GPIO3
3	gpio3_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on GPIO3 1: Un-mask CH4 over current fault report on GPIO3
2	gpio3_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on GPIO3 1: Un-mask CH3 over current fault report on GPIO3
1	gpio3_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on GPIO3 1: Un-mask CH2 over current fault report on GPIO3
0	gpio3_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on GPIO3 1: Un-mask CH1 over current fault report on GPIO3

9.2.2.63 DIG_FAULT_GPIO3_SEL3 (Page 1,Offset=6Eh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio3_clip_ch4_sel	gpio3_clip_ch3_sel	gpio3_clip_ch2_sel	gpio3_clip_ch1_sel	gpio3_otw_ch4_sel	gpio3_otw_ch3_sel	gpio3_otw_ch2_sel	gpio3_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio3_clip_ch4_sel	R/W	1	0: Mask CH4 clip on GPIO3 1: Un-mask CH4 dc fault report on GPIO3
6	gpio3_clip_ch3_sel	R/W	1	0: Mask CH3 clip on GPIO3 1: Un-mask CH3 dc fault report on GPIO3
5	gpio3_clip_ch2_sel	R/W	1	0: Mask CH2 clip on GPIO3 1: Un-mask CH2 dc fault report on GPIO3
4	gpio3_clip_ch1_sel	R/W	1	0: Mask CH1 clip on GPIO3 1: Un-mask CH1 dc fault report on GPIO3
3	gpio3_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on GPIO3 1: Un-mask CH4 OT warning report on GPIO3
2	gpio3_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on GPIO3 1: Un-mask CH3 OT warning report on GPIO3
1	gpio3_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on GPIO3 1: Un-mask CH2 OT warning report on GPIO3
0	gpio3_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on GPIO3 1: Un-mask CH1 OT warning report on GPIO3

9.2.2.64 DIG_FAULT_GPIO3_SEL4 (Page 1,Offset=6Fh) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio3_cbc_warn_ch4_sel	gpio3_cbc_warn_ch3_sel	gpio3_cbc_warn_ch2_sel	gpio3_cbc_warn_ch1_sel	gpio3_cbc_fault_ch4_sel	gpio3_cbc_fault_ch3_sel	gpio3_cbc_fault_ch2_sel	gpio3_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio3_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on GPIO3 1: Un-mask CH4 CBC warning report on GPIO3
6	gpio3_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on GPIO3 1: Un-mask CH3 CBC warning report on GPIO3
5	gpio3_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on GPIO3 1: Un-mask CH2 CBC warning report on GPIO3
4	gpio3_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on GPIO3 1: Un-mask CH1 CBC warning report on GPIO3
3	gpio3_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on GPIO3 1: Un-mask CH4 CBC fault report on GPIO3
2	gpio3_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on GPIO3 1: Un-mask CH3 CBC fault report on GPIO3
1	gpio3_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on GPIO3 1: Un-mask CH2 CBC fault report on GPIO3

Bit	Field	Type	Reset	Description
0	gpio3_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on GPIO3 1: Un-mask CH1 CBC fault report on GPIO3

9.2.2.65 DIG_FAULT_GPIO3_SEL5 (Page 1,Offset=70h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio3_rtdg_ol_det_ch4_sel	gpio3_rtdg_ol_det_ch3_sel	gpio3_rtdg_ol_det_ch2_sel	gpio3_rtdg_ol_det_ch1_sel	gpio3_rtdg_sl_det_ch4_sel	gpio3_rtdg_sl_det_ch3_sel	gpio3_rtdg_sl_det_ch2_sel	gpio3_rtdg_sl_det_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio3_rtdg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on GPIO3 1: Un-mask CH4 real-time open load on GPIO3
6	gpio3_rtdg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on GPIO3 1: Un-mask CH3 real-time open load on GPIO3
5	gpio3_rtdg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on GPIO3 1: Un-mask CH2 real-time open load on GPIO3
4	gpio3_rtdg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on GPIO3 1: Un-mask CH1 real-time open load on GPIO3
3	gpio3_rtdg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on GPIO3 1: Un-mask CH4 real-time short load on GPIO3
2	gpio3_rtdg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on GPIO3 1: Un-mask CH3 real-time short load on GPIO3
1	gpio3_rtdg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on GPIO3 1: Un-mask CH2 real-time short load on GPIO3
0	gpio3_rtdg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on GPIO3 1: Un-mask CH1 real-time short load on GPIO3

9.2.2.66 DIG_FAULT_GPIO4_SEL1 (Page 1,Offset=71h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio4_clk_fault_sel	gpio4_pvdd_uv_sel	gpio4_pvdd_ov_sel	gpio4_otstd_global_sel	gpio4_otstd_ch4_sel	gpio4_otstd_ch3_sel	gpio4_otstd_ch2_sel	gpio4_otstd_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio4_clk_fault_sel	R/W	1	0: Mask clock fault report on GPIO4 1: Un-mask clock fault report on GPIO4
6	gpio4_pvdd_uv_sel	R/W	1	0: Mask PVDD under voltage fault report on GPIO4 1: Un-mask PVDD under voltage fault report on GPIO4
5	gpio4_pvdd_ov_sel	R/W	1	0: Mask PVDD over voltage fault report on GPIO4 1: Un-mask PVDD over voltage fault report on GPIO4
4	gpio4_otstd_global_sel	R/W	1	0: Mask global over temperature shutdown fault report on GPIO4 1: Un-mask global over temperature shutdown fault report on GPIO4
3	gpio4_otstd_ch4_sel	R/W	1	0: Mask CH4 over temperature shutdown fault report on GPIO4 1: Un-mask CH4 over temperature shutdown fault report on GPIO4
2	gpio4_otstd_ch3_sel	R/W	1	0: Mask CH3 over temperature shutdown fault report on GPIO4 1: Un-mask CH3 over temperature shutdown fault report on GPIO4
1	gpio4_otstd_ch2_sel	R/W	1	0: Mask CH2 over temperature shutdown fault report on GPIO4 1: Un-mask CH2 over temperature shutdown fault report on GPIO4
0	gpio4_otstd_ch1_sel	R/W	1	0: Mask CH1 over temperature shutdown fault report on GPIO4 1: Un-mask CH1 over temperature shutdown fault report on GPIO4

9.2.2.67 DIG_FAULT_GPIO4_SEL2 (Page 1,Offset=72h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio4_dc_ch4_sel	gpio4_dc_ch3_sel	gpio4_dc_ch2_sel	gpio4_dc_ch1_sel	gpio4_oc_ch4_sel	gpio4_oc_ch3_sel	gpio4_oc_ch2_sel	gpio4_oc_ch1_sel

Bit	Field	Type	Reset	Description
7	gpio4_dc_ch4_sel	R/W	1	0: Mask CH4 dc fault report on GPIO4 1: Un-mask CH4 dc fault report on GPIO4
6	gpio4_dc_ch3_sel	R/W	1	0: Mask CH3 dc fault report on GPIO4 1: Un-mask CH3 dc fault report on GPIO4
5	gpio4_dc_ch2_sel	R/W	1	0: Mask CH2 dc fault report on GPIO4 1: Un-mask CH2 dc fault report on GPIO4
4	gpio4_dc_ch1_sel	R/W	1	0: Mask CH1 dc fault report on GPIO4 1: Un-mask CH1 dc fault report on GPIO4
3	gpio4_oc_ch4_sel	R/W	1	0: Mask CH4 over current fault report on GPIO4 1: Un-mask CH4 over current fault report on GPIO4
2	gpio4_oc_ch3_sel	R/W	1	0: Mask CH3 over current fault report on GPIO4 1: Un-mask CH3 over current fault report on GPIO4
1	gpio4_oc_ch2_sel	R/W	1	0: Mask CH2 over current fault report on GPIO4 1: Un-mask CH2 over current fault report on GPIO4
0	gpio4_oc_ch1_sel	R/W	1	0: Mask CH1 over current fault report on GPIO4 1: Un-mask CH1 over current fault report on GPIO4

9.2.2.68 DIG_FAULT_GPIO4_SEL3 (Page 1, Offset=73h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio4_clip_ch4_sel	gpio4_clip_ch3_sel	gpio4_clip_ch2_sel	gpio4_clip_ch1_sel	gpio4_otw_ch4_sel	gpio4_otw_ch3_sel	gpio4_otw_ch2_sel	gpio4_otw_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio4_clip_ch4_sel	R/W	1	0: Mask CH4 clip on GPIO4 1: Un-mask CH4 dc fault report on GPIO4
6	gpio4_clip_ch3_sel	R/W	1	0: Mask CH3 clip on GPIO4 1: Un-mask CH3 dc fault report on GPIO4
5	gpio4_clip_ch2_sel	R/W	1	0: Mask CH2 clip on GPIO4 1: Un-mask CH2 dc fault report on GPIO4
4	gpio4_clip_ch1_sel	R/W	1	0: Mask CH1 clip on GPIO4 1: Un-mask CH1 dc fault report on GPIO4
3	gpio4_otw_ch4_sel	R/W	1	0: Mask CH4 OT warning report on GPIO4 1: Un-mask CH4 OT warning report on GPIO4
2	gpio4_otw_ch3_sel	R/W	1	0: Mask CH3 OT warning report on GPIO4 1: Un-mask CH3 OT warning report on GPIO4
1	gpio4_otw_ch2_sel	R/W	1	0: Mask CH2 OT warning report on GPIO4 1: Un-mask CH2 OT warning report on GPIO4
0	gpio4_otw_ch1_sel	R/W	1	0: Mask CH1 OT warning report on GPIO4 1: Un-mask CH1 OT warning report on GPIO4

9.2.2.69 DIG_FAULT_GPIO4_SEL4 (Page 1, Offset=74h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio4_cbc_warn_ch4_sel	gpio4_cbc_warn_ch3_sel	gpio4_cbc_warn_ch2_sel	gpio4_cbc_warn_ch1_sel	gpio4_cbc_fault_ch4_sel	gpio4_cbc_fault_ch3_sel	gpio4_cbc_fault_ch2_sel	gpio4_cbc_fault_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio4_cbc_warn_ch4_sel	R/W	1	0: Mask CH4 CBC warning report on GPIO4 1: Un-mask CH4 CBC warning report on GPIO4
6	gpio4_cbc_warn_ch3_sel	R/W	1	0: Mask CH3 CBC warning report on GPIO4 1: Un-mask CH3 CBC warning report on GPIO4
5	gpio4_cbc_warn_ch2_sel	R/W	1	0: Mask CH2 CBC warning report on GPIO4 1: Un-mask CH2 CBC warning report on GPIO4
4	gpio4_cbc_warn_ch1_sel	R/W	1	0: Mask CH1 CBC warning report on GPIO4 1: Un-mask CH1 CBC warning report on GPIO4
3	gpio4_cbc_fault_ch4_sel	R/W	1	0: Mask CH4 CBC fault report on GPIO4 1: Un-mask CH4 CBC fault report on GPIO4

Bit	Field	Type	Reset	Description
2	gpio4_cbc_fault_ch3_sel	R/W	1	0: Mask CH3 CBC fault report on GPIO4 1: Un-mask CH3 CBC fault report on GPIO4
1	gpio4_cbc_fault_ch2_sel	R/W	1	0: Mask CH2 CBC fault report on GPIO4 1: Un-mask CH2 CBC fault report on GPIO4
0	gpio4_cbc_fault_ch1_sel	R/W	1	0: Mask CH1 CBC fault report on GPIO4 1: Un-mask CH1 CBC fault report on GPIO4

9.2.2.70 DIG_FAULT_GPIO4_SEL5 (Page 1, Offset=75h) [Reset=0xFF]

7	6	5	4	3	2	1	0
gpio4_rtlldg_ol_det_ch4_sel	gpio4_rtlldg_ol_det_ch3_sel	gpio4_rtlldg_ol_det_ch2_sel	gpio4_rtlldg_ol_det_ch1_sel	gpio4_rtlldg_sl_det_ch4_sel	gpio4_rtlldg_sl_det_ch3_sel	gpio4_rtlldg_sl_det_ch2_sel	gpio4_rtlldg_sl_det_ch1_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	gpio4_rtlldg_ol_det_ch4_sel	R/W	1	0: Mask CH4 real-time open load on GPIO4 1: Un-mask CH4 real-time open load on GPIO4
6	gpio4_rtlldg_ol_det_ch3_sel	R/W	1	0: Mask CH3 real-time open load on GPIO4 1: Un-mask CH3 real-time open load on GPIO4
5	gpio4_rtlldg_ol_det_ch2_sel	R/W	1	0: Mask CH2 real-time open load on GPIO4 1: Un-mask CH2 real-time open load on GPIO4
4	gpio4_rtlldg_ol_det_ch1_sel	R/W	1	0: Mask CH1 real-time open load on GPIO4 1: Un-mask CH1 real-time open load on GPIO4
3	gpio4_rtlldg_sl_det_ch4_sel	R/W	1	0: Mask CH4 real-time short load on GPIO4 1: Un-mask CH4 real-time short load on GPIO4
2	gpio4_rtlldg_sl_det_ch3_sel	R/W	1	0: Mask CH3 real-time short load on GPIO4 1: Un-mask CH3 real-time short load on GPIO4
1	gpio4_rtlldg_sl_det_ch2_sel	R/W	1	0: Mask CH2 real-time short load on GPIO4 1: Un-mask CH2 real-time short load on GPIO4
0	gpio4_rtlldg_sl_det_ch1_sel	R/W	1	0: Mask CH1 real-time short load on GPIO4 1: Un-mask CH1 real-time short load on GPIO4

9.2.2.71 DIG_IO_OPENDRAIN_EN (Page 1, Offset=76h) [Reset=0x3F]

7	6	5	4	3	2	1	0
Reserved		gpio4_classh_opendrain_en	gpio3_classh_opendrain_en	gpio2_classh_opendrain_en	gpio1_classh_opendrain_en	gpio0_classh_opendrain_en	sdout_classh_opendrain_en
R/W		R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	Reserved
5	gpio4_classh_opendrain_en	R/W	1	0: Set GPIO4 as Push-pull for Class-H operation 1: Set GPIO4 as Open-drain for Class-H operation
4	gpio3_classh_opendrain_en	R/W	1	0: Set GPIO3 as Push-pull for Class-H operation 1: Set GPIO3 as Open-drain for Class-H operation
3	gpio2_classh_opendrain_en	R/W	1	0: Set GPIO2 as Push-pull for Class-H operation 1: Set GPIO2 as Open-drain for Class-H operation
2	gpio1_classh_opendrain_en	R/W	1	0: Set GPIO1 as Push-pull for Class-H operation 1: Set GPIO1 as Open-drain for Class-H operation
1	gpio0_classh_opendrain_en	R/W	1	0: Set GPIO0 as Push-pull for Class-H operation 1: Set GPIO0 as Open-drain for Class-H operation
0	sdout_classh_opendrain_en	R/W	1	0: Set SDOUT as Push-pull for Class-H operation 1: Set SDOUT as Open-drain for Class-H operation

9.2.2.72 DIG_IO_GVDD_FAULT_SEL (Page 1, Offset=77h) [Reset=0x3F]

7	6	5	4	3	2	1	0
Reserved		gpio4_gvdd_fault_sel	gpio3_gvdd_fault_sel	gpio2_gvdd_fault_sel	gpio1_gvdd_fault_sel	gpio0_gvdd_fault_sel	sdout_gvdd_fault_sel
R/W		R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	Reserved
5	gpio4_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on GPIO4 1: Un-mask GVDD fault report on GPIO4
4	gpio3_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on GPIO3 1: Un-mask GVDD fault report on GPIO3
3	gpio2_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on GPIO2 1: Un-mask GVDD fault report on GPIO2
2	gpio1_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on GPIO1 1: Un-mask GVDD fault report on GPIO1
1	gpio0_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on GPIO0 1: Un-mask GVDD fault report on GPIO0
0	sdout_gvdd_fault_sel	R/W	1	0: Mask GVDD fault report on SDOUT 1: Un-mask GVDD fault report on SDOUT

9.2.2.73 DIG_IO_OTW_GLOBAL_SEL (Page 1,Offset=78h) [Reset=0x3F]

7	6	5	4	3	2	1	0
otsd_fault_latch_sel	Reserved	gpio4_otw_global_sel	gpio3_otw_global_sel	gpio2_otw_global_sel	gpio1_otw_global_sel	gpio0_otw_global_sel	sdout_otw_global_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	otsd_fault_latch_sel	R/W	0	0: OTSD fault non-latch on GPIO 1: OTSD fault report latch on GPIO
6	Reserved	R/W	0	Reserved
5	gpio4_otw_global_sel	R/W	1	0: Mask global OT warning report on GPIO4 1: Un-mask global OT warning report on GPIO4
4	gpio3_otw_global_sel	R/W	1	0: Mask global OT warning report on GPIO3 1: Un-mask global OT warning report on GPIO3
3	gpio2_otw_global_sel	R/W	1	0: Mask global OT warning report on GPIO2 1: Un-mask global OT warning report on GPIO2
2	gpio1_otw_global_sel	R/W	1	0: Mask global OT warning report on GPIO1 1: Un-mask global OT warning report on GPIO1
1	gpio0_otw_global_sel	R/W	1	0: Mask global OT warning report on GPIO0 1: Un-mask global OT warning report on GPIO0
0	sdout_otw_global_sel	R/W	1	0: Mask global OT warning report on SDOUT 1: Un-mask global OT warning report on SDOUT

9.2.2.74 DIG_DC_DIAG_FAULT_SEL (Page 1,Offset=79h) [Reset=0x30]

7	6	5	4	3	2	1	0
Reserved	gpio4_dc_diag_fault_sel	gpio3_dc_diag_fault_sel	gpio2_dc_diag_fault_sel	gpio1_dc_diag_fault_sel	gpio0_dc_diag_fault_sel	sdout_dc_diag_fault_sel	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	00	Reserved
5	gpio4_dc_diag_fault_sel	R/W	1	0: Mask DC load diagnostic fault report on GPIO4 1: Un-mask DC load diagnostic fault report on GPIO4
4	gpio3_dc_diag_fault_sel	R/W	1	0: Mask DC load diagnostic fault report on GPIO3 1: Un-mask DC load diagnostic fault report on GPIO3
3	gpio2_dc_diag_fault_sel	R/W	0	0: Mask DC load diagnostic fault report on GPIO2 1: Un-mask DC load diagnostic fault report on GPIO2
2	gpio1_dc_diag_fault_sel	R/W	0	0: Mask DC load diagnostic fault report on GPIO1 1: Un-mask DC load diagnostic fault report on GPIO1
1	gpio0_dc_diag_fault_sel	R/W	0	0: Mask DC load diagnostic fault report on GPIO0 1: Un-mask DC load diagnostic fault report on GPIO0
0	sdout_dc_diag_fault_sel	R/W	0	0: Mask DC load diagnostic fault report on SDOUT 1: Un-mask DC load diagnostic fault report on SDOUT

9.2.2.1 DIG_FAULT_LATCH_SEL (Page 1,Offset=80h) [Reset=0xF0]

7	6	5	4	3	2	1	0

dc_diag_fault_latch_sel	rtldg_ol_fault_latch_sel	rtldg_sl_fault_latch_sel	cbc_fault_latch_sel	cbc_warn_latch_sel	clk_err_fault_latch_sel	clip_latch_sel	otw_latch_sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	dc_diag_fault_latch_sel	R/W	1	0: DC load diagnostic fault report non-latch on GPIO 1: DC load diagnostic fault report latch on GPIO
6	rtldg_ol_fault_latch_sel	R/W	1	0: Real-time open-load fault report non-latch on GPIO 1: Real-time open-load fault report latch on GPIO
5	rtldg_sl_fault_latch_sel	R/W	1	0: Real-time short-load fault report non-latch on GPIO 1: Real-time short-load fault report latch on GPIO
4	cbc_fault_latch_sel	R/W	1	0: CBC fault report non-latch on GPIO 1: CBC fault report latch on GPIO
3	cbc_warn_latch_sel	R/W	0	0: CBC warning report non-latch on GPIO 1: CBC warning report latch on GPIO
2	clk_err_fault_latch_sel	R/W	0	0: Clock error fault report non-latch on GPIO 1: Clock error fault report latch on GPIO
1	clip_latch_sel	R/W	0	0: Clip report non-latch on GPIO 1: Clip report latch on GPIO
0	otw_latch_sel	R/W	0	0: OT warning report non-latch on GPIO 1: OT warning report latch on GPIO

10. Application Information

10.1 BTL Application

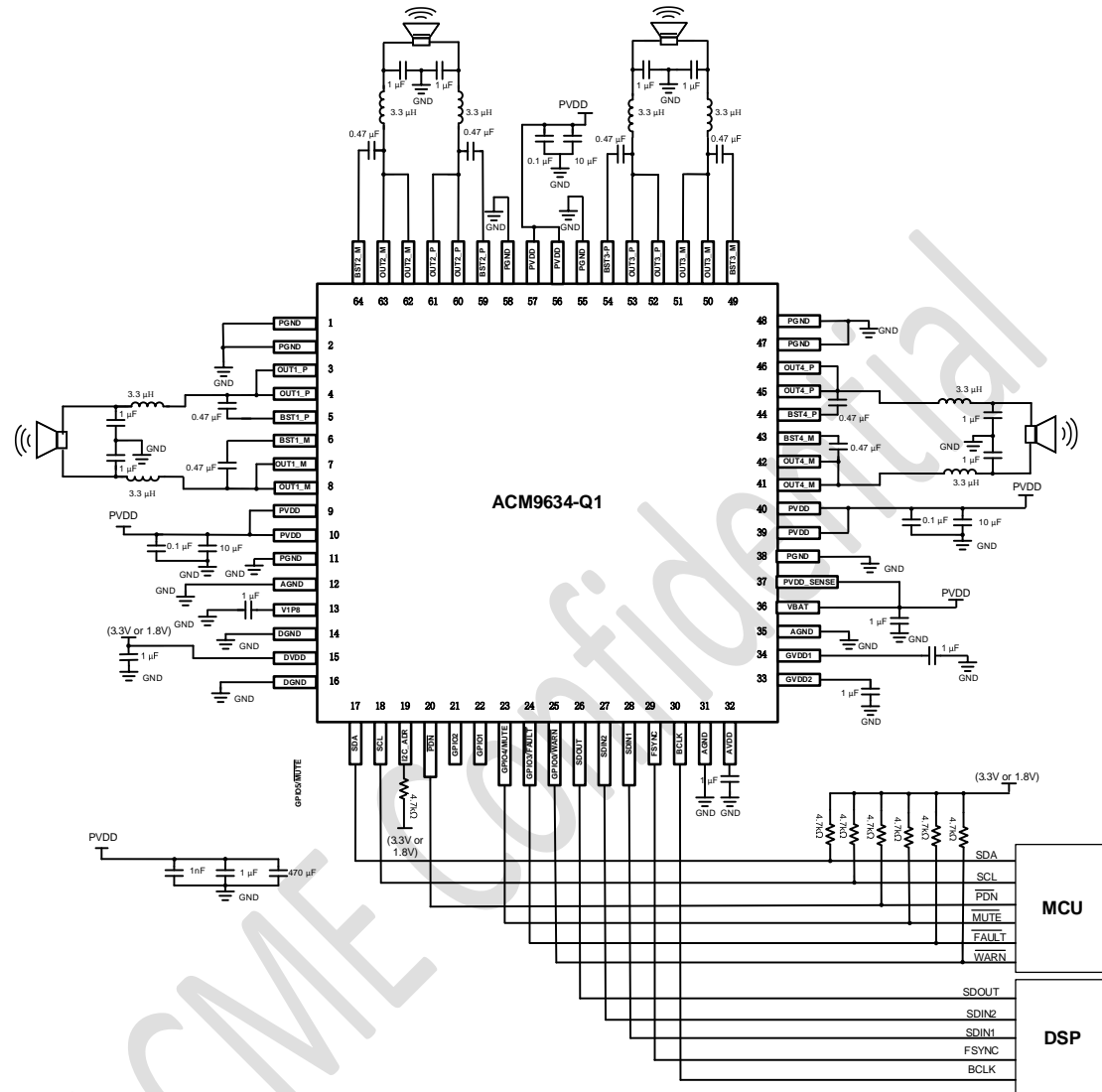


Figure 10-1. Typical Application Circuit – BTL

11.1.2 Detail Layout Guidelines

The ACM9634-Q1 Demo Board is designed with the consideration of low EMI and good audio performance. As the ACM9634-Q1 has an exposed thermal pad on the top of the package, a heatsink must be included in the layout.

Please refer to Figure 11-1 for the following guidelines,

- A. As all the high current path are on the top layer, an integrated GND plane on the second layer helps to reduce the EMI by providing a low impedance return path for high frequency noise.
- B. The decoupling capacitors on PVDD, should be placed very close to the device PVDD/GND pins, and maintain a minimum loop area among PVDD/GND/decoupling capacitor. Also, vias are not recommended along this loop.
- C. The decoupling capacitors for GVDD/AVDD/V1P8 should also be placed on the same layer with the device and as close as possible to the related pins.
- D. The ground connections for the capacitors in the LC filter, should have a direct path back to the device and the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection.
- E. The traces from the output pins to the inductors should have the shortest trace possible to allow for the smallest loop of large switching currents.
- F. Heat-sink mounting screws should be close to the device to keep the loop short from the package to ground.
- G. Many vias stitching together the ground planes can create a shield to isolate the amplifier and power supply.

11.2 Layout Example

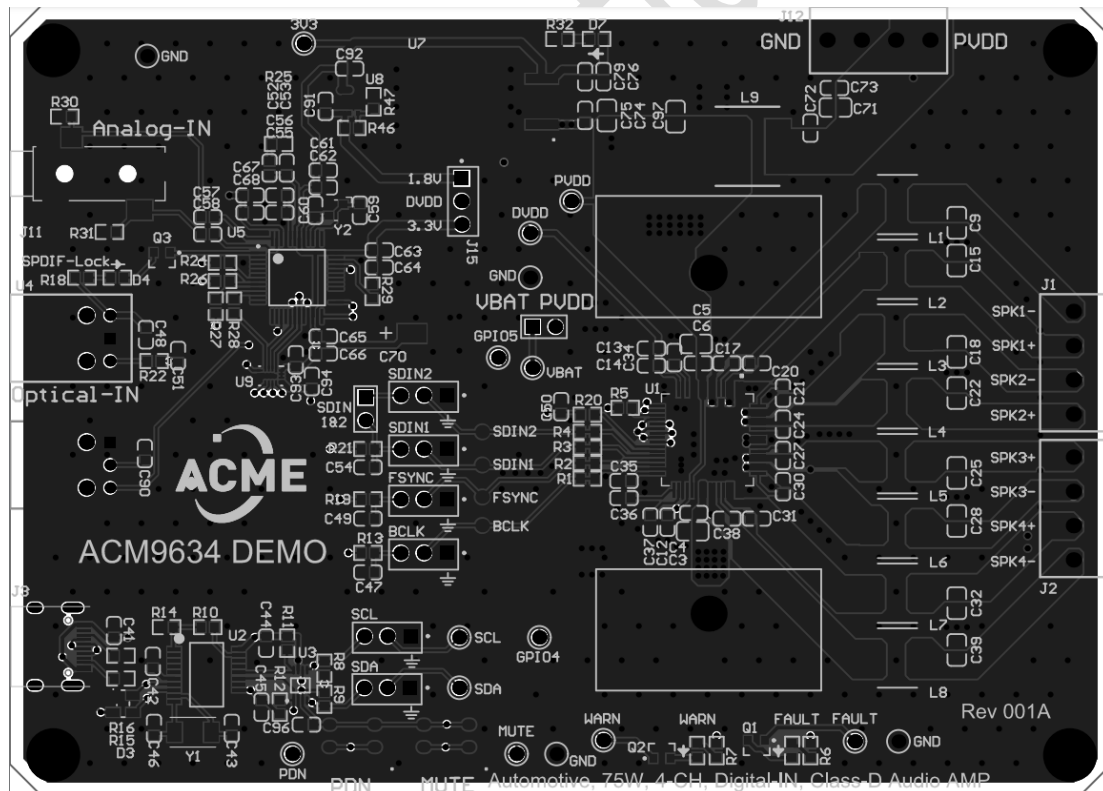
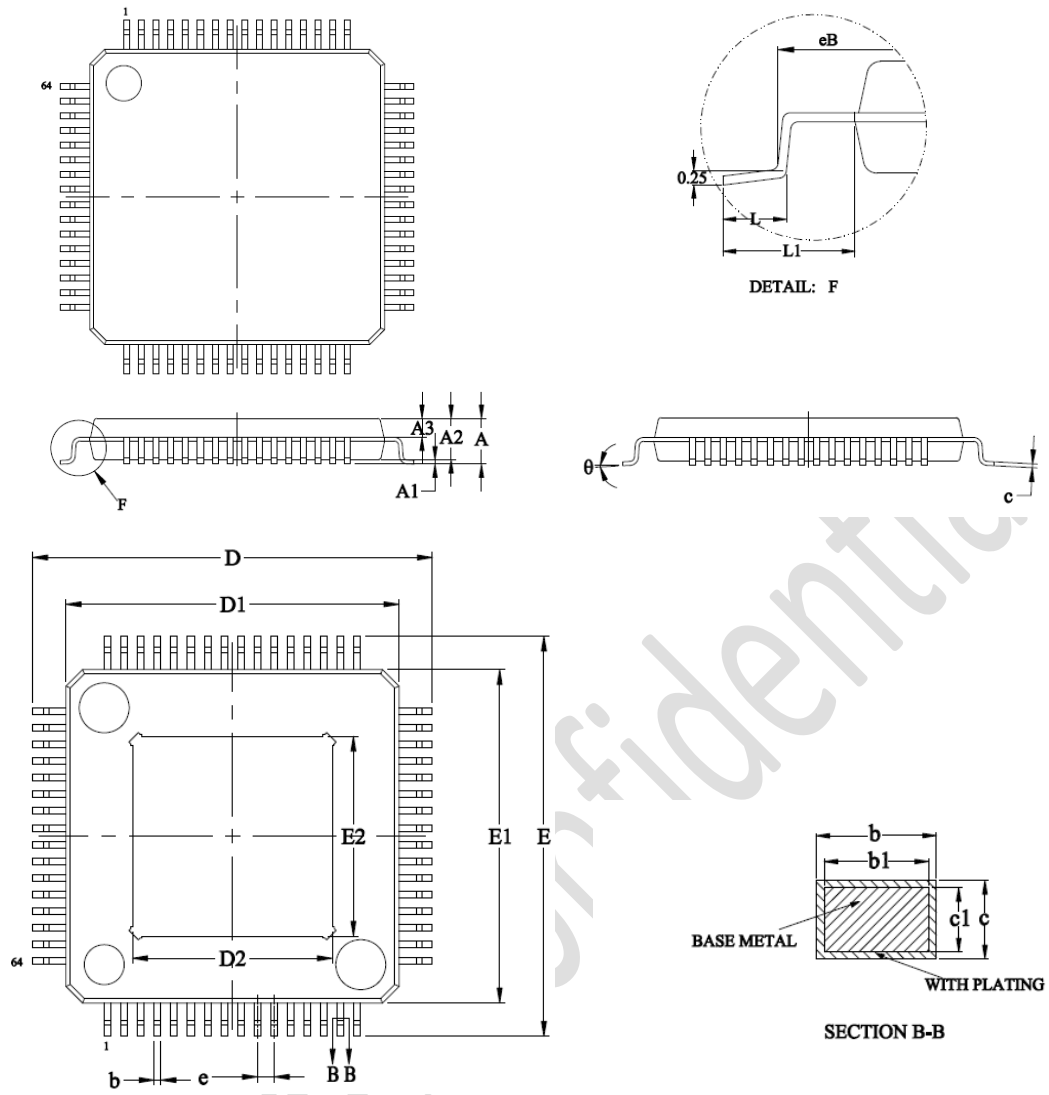


Figure 11-1. ACM9634-Q1 Demo Board Layout

12. Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

L/F SIZE (mil)	SIZE (mm)	D2	E2
244×244		6.00REF	6.00REF

Revision History

Change from the preliminary version to full version (Nov 2023)

Full version datasheet released.

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