ACM1201M Stereo, 192KHz PDM Audio ADC

1. Features

- **Single Supply Voltage**
  - AVDD= 3.0 – 5.5V (typ. 3.3V)
- **Audio ADC Performance**
  - Stereo Audio ADC
  - Differential-ended Input
- **Excellent Audio Performance**
  - THD: typical 90dB
  - Dynamic Range: typical 92dB
  - SNR: typical 92dB
- **Gain Support**
  - 6dBFS/V
  - 12dBFS/V
  - 17dBFS/V
- **Audio Interface Format**
  - PDM interface
- **Sample Rate Support**
  - 8kHz - 192kHz

2. Applications

- Microphone array ADC
- Conference System voice capture
- Smart Speaker
- AV Recorder
- Audio IOT device

3. General Description

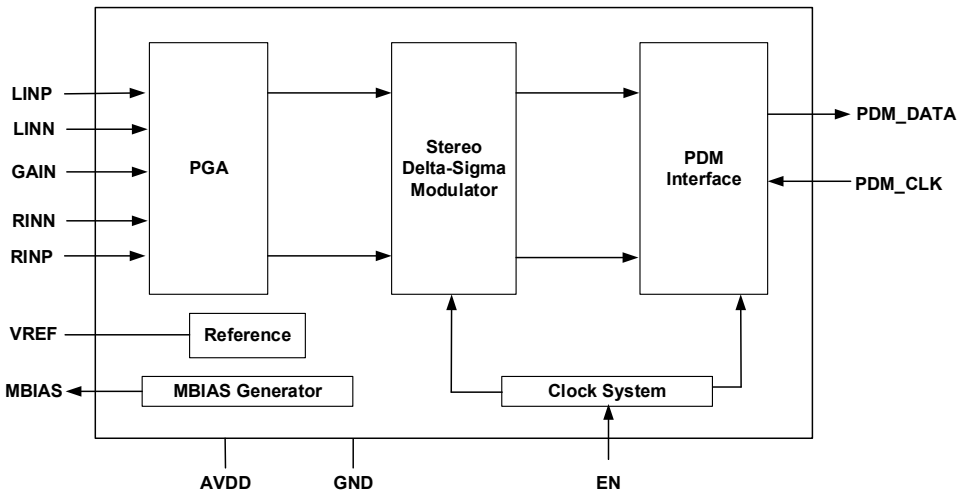
The ACM1201M device is a high performance, low cost, single chip, stereo analog-to-digital converter with differential-ended analog voltage input. The ACM1201M device uses a delta-sigma modulator with PGA. For various applications, the ACM1201M device supports 8k to 192K maximum sample rate with 6.144MHz PDM clock input. The ACM1201M device supports the low power and idle functions by means of low frequency of PDM clock input and halting the PDM clock.

The ACM1201M device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5V or 3.3V analog supply. The device is available in a small 2.5mm x 2.5mm QFN 12 package.

4. Device Information

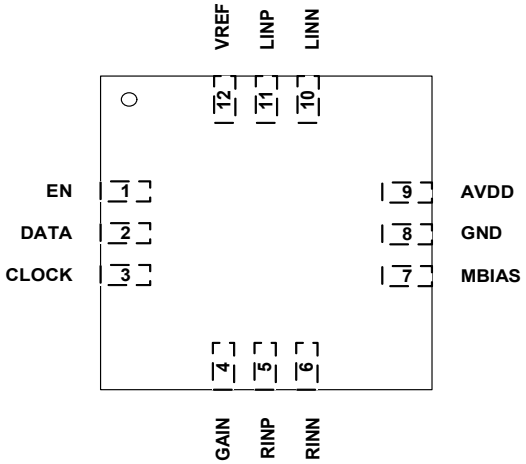
Part number	Package	Body size
ACM1201M	QFN 12	*2.5 mm × 2.5 m*m

ACM1201M Block Diagram



5. Pin Configuration and Function Descriptions

ACM1201M
Top View



Pin No.	Name	Type	Description
1	EN	AIN	Enable, high=active
2	DATA	DO	PDM Data
3	CLOCK	DI	PDM Clock
4	GAIN	AIN	Gain selection, high=17dBFS/V, low=6dBFS/V, floating=12dBFS/V
5	RINP	AIN	Positive audio input of right channel
6	RINN	AIN	Negative audio input of right channel
7	MBIAS	AOUT	Microphone Bias Output (2.8V)
8	GND	PWR	Ground
9	AVDD	PWR	Power supply
10	LINN	AIN	Negative audio input of right channel
11	LINP	AIN	Positive audio input of left channel
12	VREF	AOUT	Voltage Reference (1.65V)

6. Specifications

6.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
AVDD	Analog power supply	-0.3	6.5	V
$V_{I(Digital)}$	AVDD referenced digital inputs (2)	-0.3	V_{AVDD}+0.3	V
$V_{I(Analog)}$	AVDD referenced analog inputs (2)	-0.3	V_{AVDD}+0.3	V
T_A	Ambient operating temperature	-40	85	℃
T_{stg}	Storage temperature	-55	150	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) AVDD referenced digital pins include: CLOCK, DATA, EN, GAIN.

6.2 ESD Ratings

			VALUE	UNIT

$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog Power Supply	3	3.3	5.5	V
V_{IH}	High input logic level	2		AVDD	V
V_{IL}	Low input logic level	0		0.8	V
V_{IH}	High input logic level	2		5.5	V
V_{IL}	Low input logic level	0		0.8	V
I_{IH}	High input logic current			+/-10	uA
I_{IL}	Low input logic current			+/-10	uA
I_{IH}	High input logic current		60	100	uA
I_{IL}	Low input logic current			+/-10	uA
V_{OH}	High output logic level	2.8		AVDD	V
V_{OL}	Low output logic level	0		0.8	V

6.4 Thermal Information

		ACM1201M QFN 12 PINS JEDEC STANDARD 4-LAYER PCB	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	TBD	℃/W
θ_{JT}	Junction-to-case (top) thermal resistance	TBD	℃/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	℃/W

6.5 Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog to Digital Converter (ADC) Performance						
Full Scale Input Signal	V_{INFS}	Gain=17dBFS/V, Input level= 115mVp		-2		dBFS
Signal to Noise Ratio	SNR	Gain=Floating, A-Weighted		92		dB
Total Harmonic Distortion	THD	Gain=Floating		90		dB
Channel Separation				100		dB
Inter channel Gain Mismatch				0.1		dB
Input Impedance				6		kΩ
DC Characteristics						
AVDD power consumption		Normal Operation		9.5		mA
Shut Down Mode		Pull EN to low			1	μA
Microphone Input & Gain						
Programmable Input Gain	GAIN Floating			12		dBFS/V
	Pull GAIN to low			6		
	Pull GAIN to high			17		
MICBIAS OUTPUT						
	MICBIAS noise			2		uVrms

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	MICBIAS voltage			2.8		V
	MICBIAS current drive			10		mA

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
PDM Audio Port Timing					
f_{CLOCK}	PDM_CLK frequency	0.512	3.072	6.144	MHz
t_{CLOCK}	PDM_CLK duty	40		60	%
t_{CLOCKL}	PDM_CLK pulse width, low	8			ns
t_{CLOCKH}	PDM_CLK pulse width, high	8			ns
t_{SU}	Data setup time, before PDM_CLK rising edge	30			ns
t_{DH}	Data hold time, after PDM_CLK rising edge	30			ns

6.7 PDM Data Timing

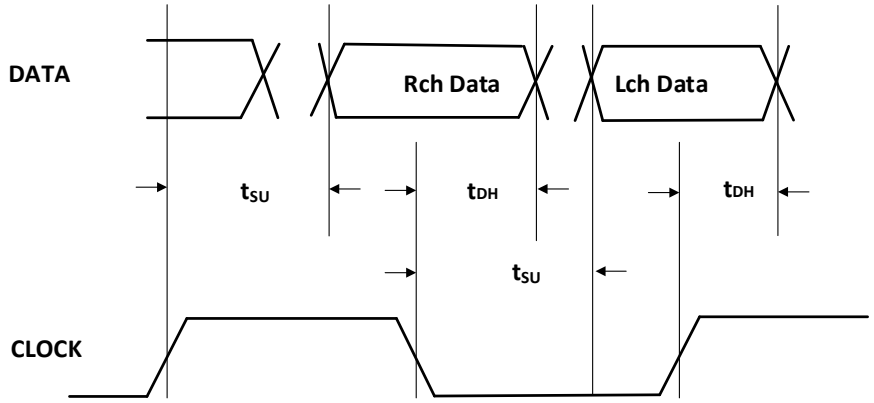
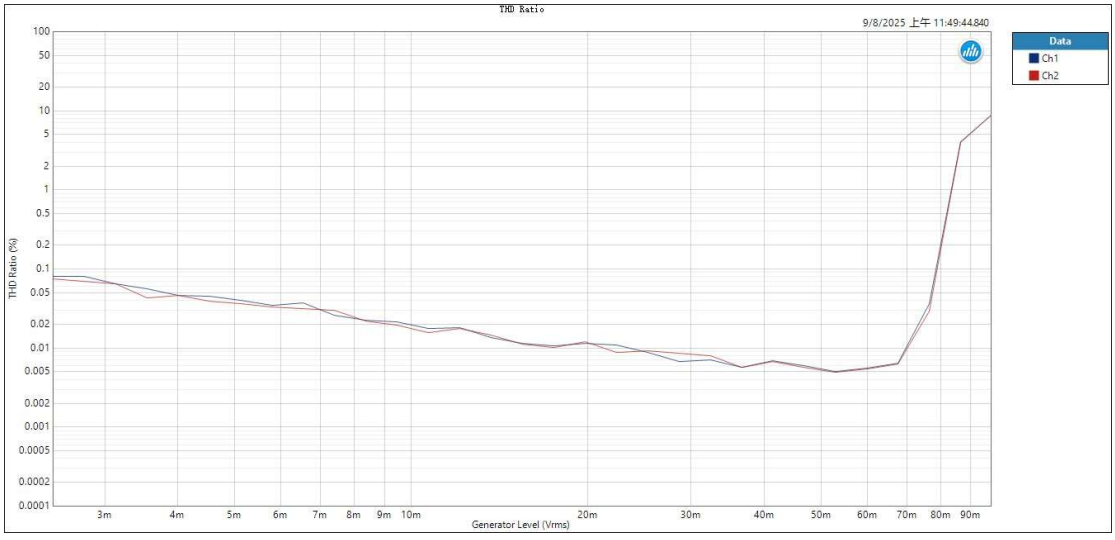


Figure 1 PDM Data Timing

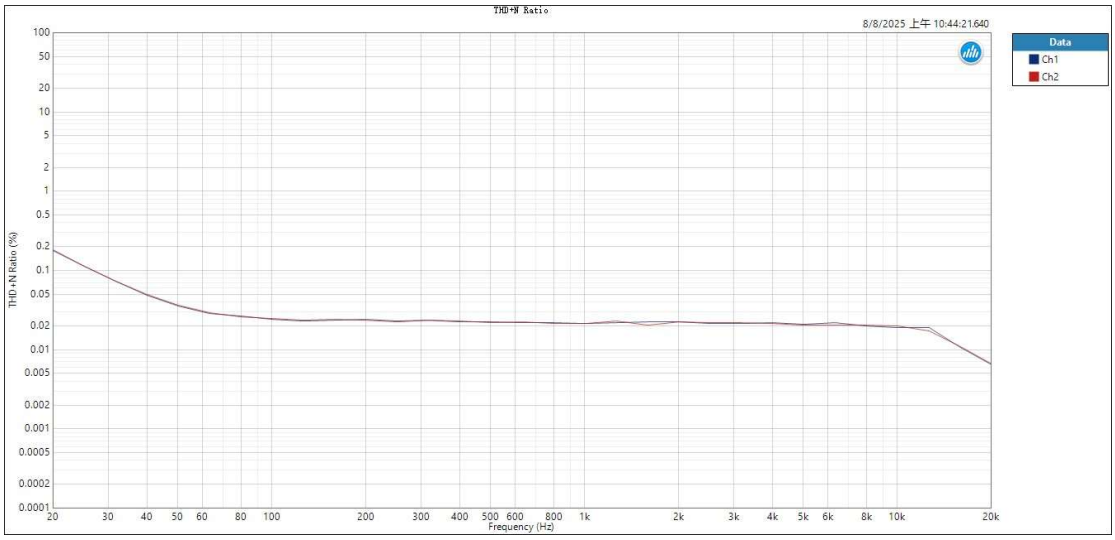
7. *Typical Characteristics*

Free-air room temperature 25℃ (unless otherwise noted). ACM1201M EVM board, AVDD=3.3V, PDM CLOCK=3.072MHz, Gain=12dBFS/V.



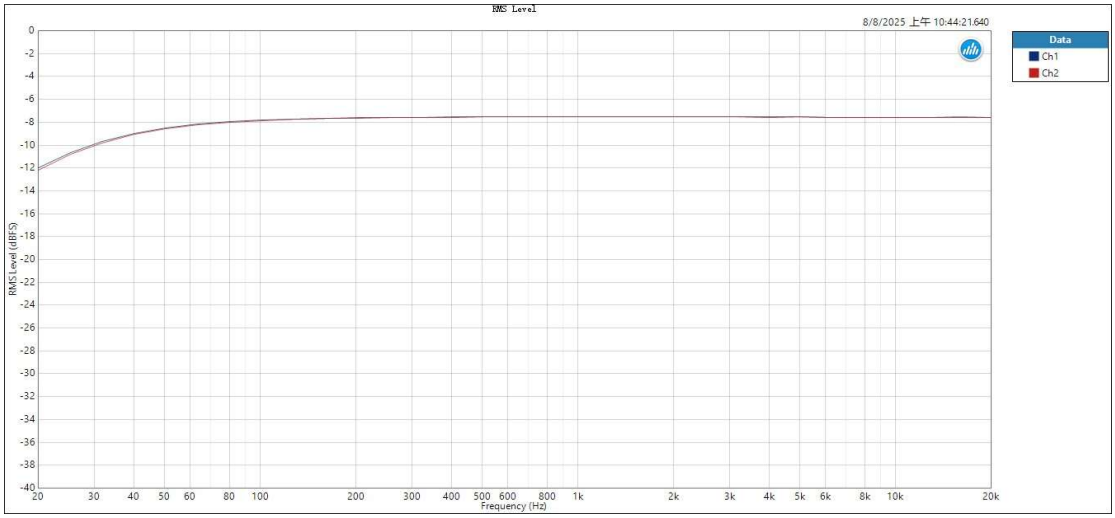
(Differential input, AVDD=3.3V, Gain=17dBFS/V)

Figure 2 THD Ratio vs Input Level



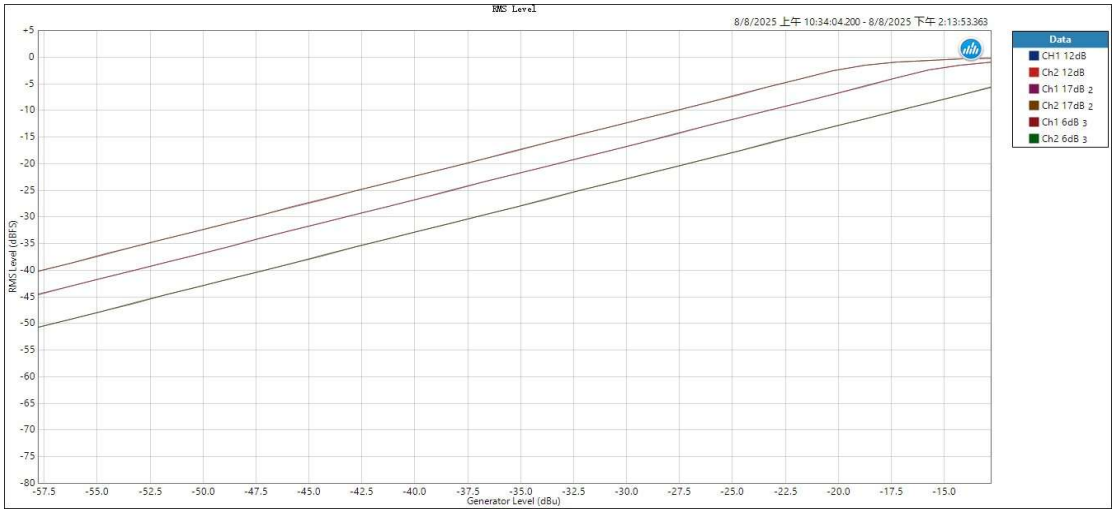
(Differential input, AVDD=3.3V, Gain=12dBFS/V)

Figure 4 THD+N vs Frequency



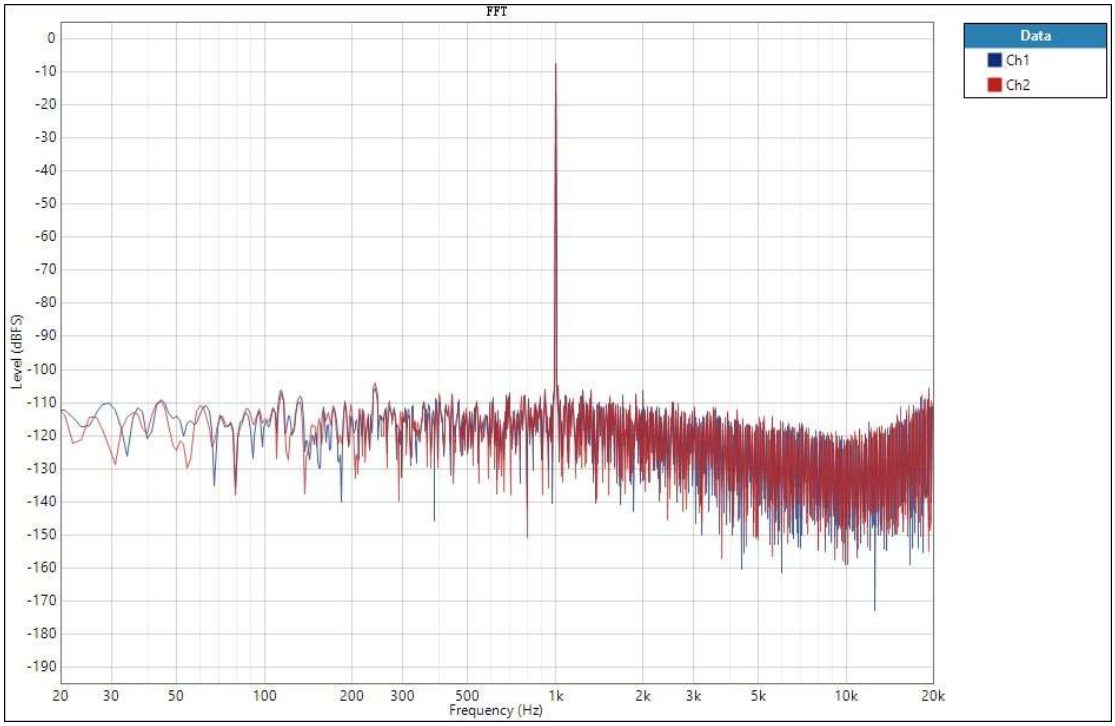
(Differential input, AVDD=3.3V, Gain=12dBFS/V)

Figure 5 Output Level vs Frequency



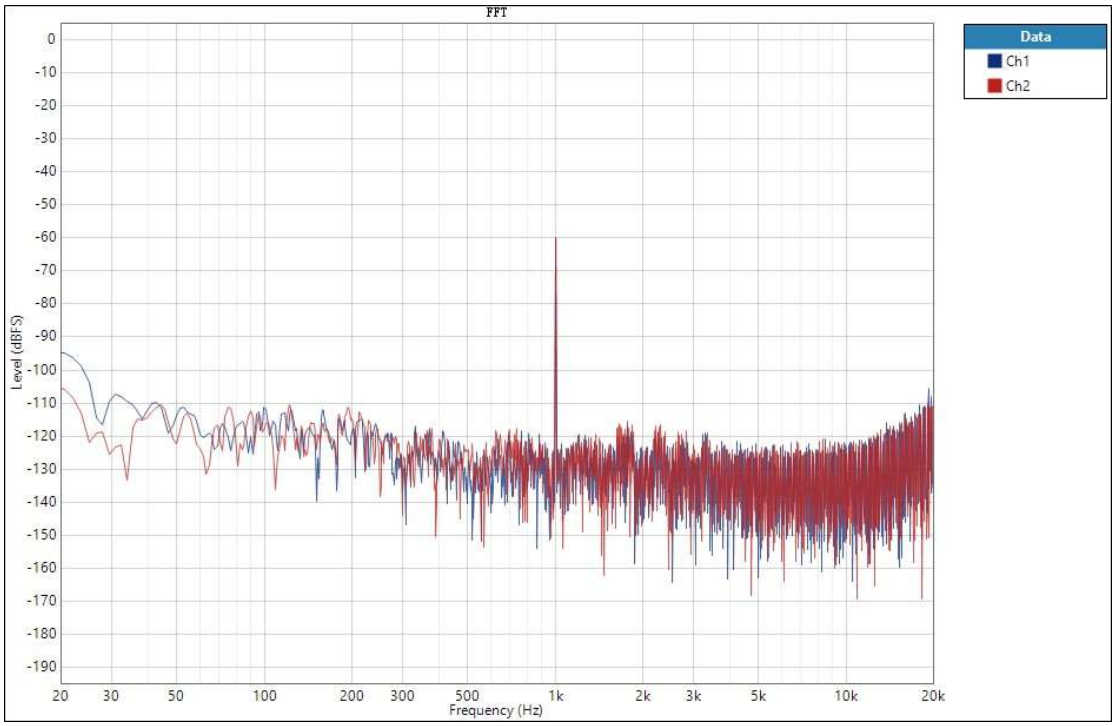
(Differential input, AVDD=3.3V)

Figure 5 Linearity



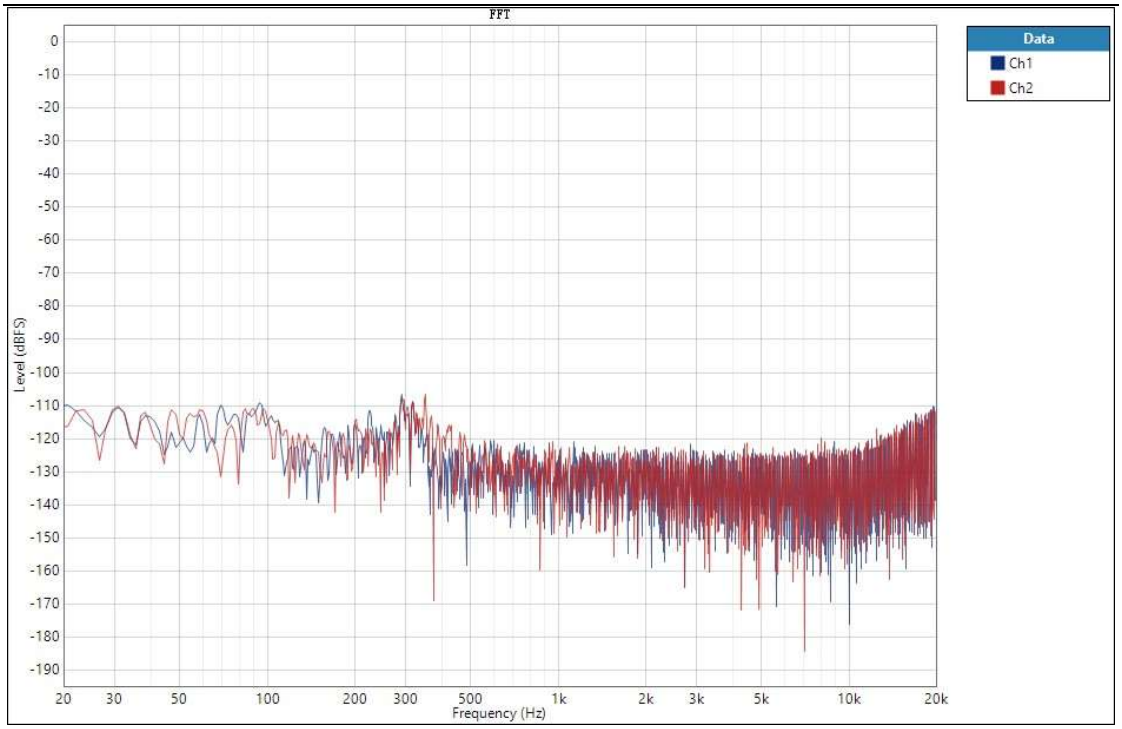
(Differential input, AVDD=3.3V, Gain=12dBFS/V)

Figure 6 FFT with -23dBV Input Level



(Differential input, AVDD=3.3V, Gain=12dBFS/V)

Figure 7 FFT with -60dBFS Output



(Differential input, AVDD=3.3V, Gain=12dBFS/V)

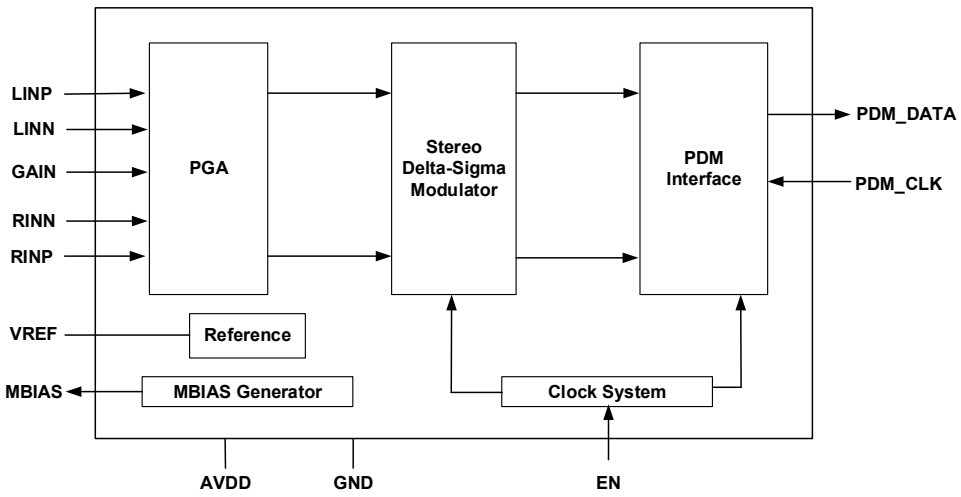
Figure 8 Noise Floor

8. Detail Description

8.1 Overview

The ACM1201M is high-performance, low-cost, single-chip, stereo analog-to-digital converter with differential-ended analog voltage input. The ACM1201M uses a delta-sigma modulator with 128-times oversampling with PGA. For various applications, the ACM1201M supports PDM in serial audio interface up to 192-kHz sampling by 6.144MHz PDM_CLOCK frequency. The ACM1201M also supports an idle function by means of halting the system clock.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1. Power On

The ACM1201M device has an internal power-on-reset circuit, and initialization (reset) occurs automatically when pulling EN pin to high. While EN is pulled to high, and PDM_CLOCK is provided after 22.5mS, the ACM1201M device digital output PDM_DATA becomes valid.

8.3.2. Serial Audio Data Interface

The ACM1201M device interfaces the audio system through PDM_CLOCK (pin 3), PDM_DATA (pin 2).

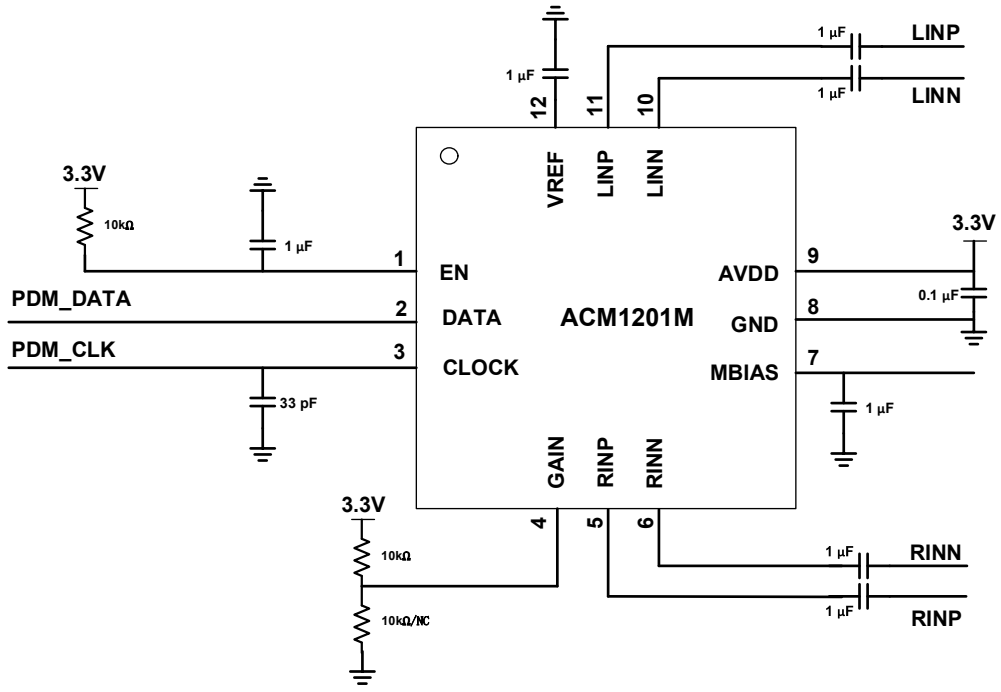
8.3.3. Clock-Halt

Halting PDM_CLOCK (pin 3), the ACM1201M enters into idle state. The function is available any time after power on. Idle state occur automatically 20uS (typical) after the halt of PDM_CLOCK. During assertion of the clock-halt, the ACM1201M device stays in the idle mode, with PDM_DATA (pin 2) forced to zero. Release the idle mode requires the supply of PDM_CLOCK. The digital output is valid after release of the idle state and elapse of 22.5mS .

8.3.4. Mode Switching

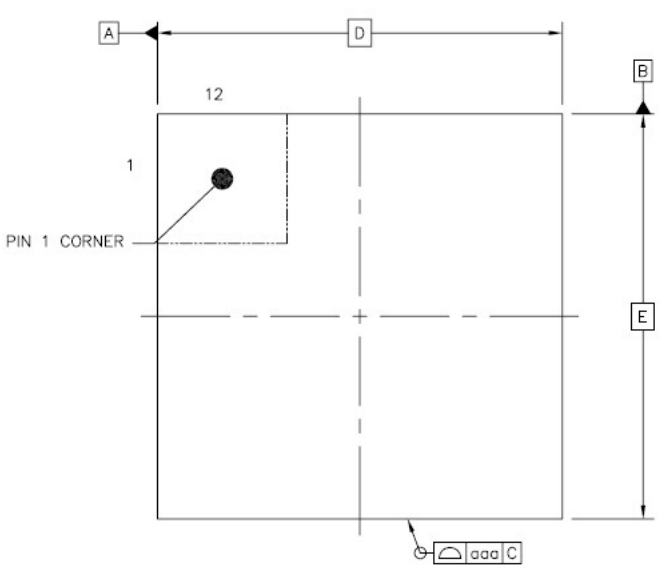
The ACM1201M device supports 3 states controlled by PDM_CLOCK. When ACM1201M is powered on, and PDM_CLOCK is not valid, the ACM1201M stay in idle mode. When PDM_CLOCK is provided (3.072MHz typical), the device enters into normal operation mode after 22.5mS. If PDM_CLOCK is <1.2MHz, the device enters into low power consumption mode. In case of low power voice wakeup application, the PDM_CLOCK changes from low frequency like 512KHz to normal 3.072MHz or 6.144MHz, the ACM1201M switches the from low power mode to normal mode within 2mS.

9. Typical Application

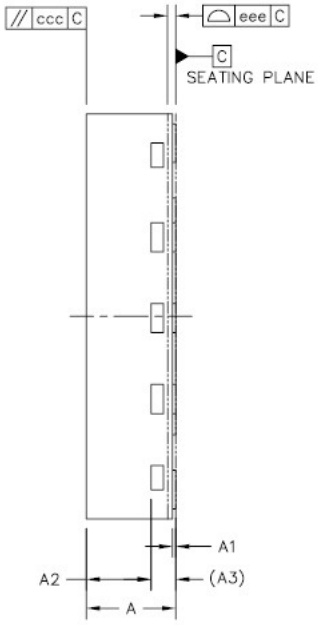


10. Package Dimensions

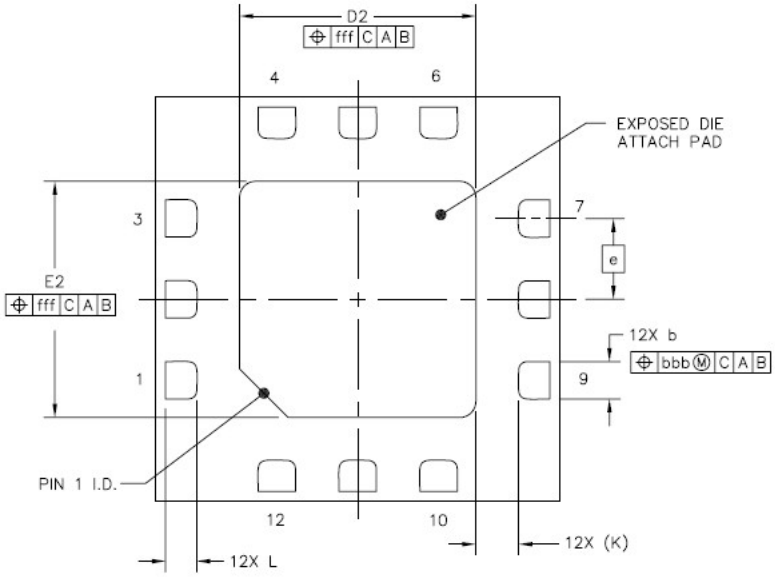
Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM1201MQFR	QFN12 Tape and Reel	5000	5000	RoHS Compliant Lead-Free Finish	MSL3	ACM1201M



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		2.5 BSC	
	Y	E		2.5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.36	1.46	1.56
	Y	E2	1.36	1.46	1.56
LEAD LENGTH		L	0.1425	0.1925	0.2425
LEAD TIP TO EXPOSED PAD EDGE		K		0.265 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

11. Revision History

Revision	Date	Description
1.0	2025.09.09	Initial version