ACM5620 21-V, 20-A, High Efficiency, Fully-integrated Synchronous Boost Converter

1. Features

- Wide input voltage and output voltage range
  - VIN : 2.7-V to 20-V
  - VOUT : 4.5-V to 21-V
- 6.5-mΩ Low-side power FET R_{DSON} and 10-mΩ High-side power FET R_{DSON}
- Low quiescent current and shutdown current
- High power capability and efficiency
  - 20-A maximum peak current limit
  - 92% efficiency at VIN = 3.6-V, VOUT = 12-V and IOUT = 2-A
  - 93% efficiency at VIN = 7.2-V, VOUT = 19-V and IOUT = 3-A
  - 95% efficiency at VIN = 10.8-V, VOUT = 19-V and IOUT = 5-A
- PFM mode in light load condition
- Programmable soft-start
- Programmable switching frequency among 300/550/800-kHz or 1MHz
- Full protection
  - Programmable current limit threshold
  - Cycle by cycle current limit
  - Overvoltage protection at 22.8-V
  - Thermal shutdown
- 3.5-mm × 3.0-mm Flip-chip QFN package

2. Applications

- Bluetooth Speaker
- E-cigarette
- Quick charge power bank

3. General Description

ACM5620 is a fully integrated, high efficiency boost converter. The low power FET ON-resistance, 6.5-mΩ for low side and 10-mΩ for high side provides high efficiency and good thermal performance. ACM5620 has a wide input voltage range of 2.7-V to 20-V and a wide output voltage range of 4.5-V to 21-V, which makes it very suitable for high output power demanding Li^+ battery applications. It can deliver over 80-W output power for 2-s Li^+ battery applications and over 120-W for 3-s Li^+ battery applications.

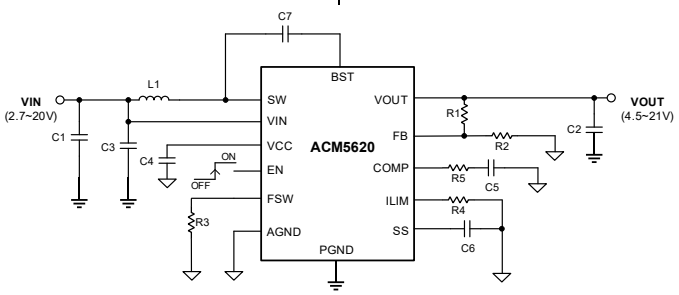
ACM5620 employs adaptive constant off-time peak current control mode to regulate the output voltage and ensure fast transient response. ACM5620 operates in the pulse width modulation (PWM) mode in moderate and heavy load condition. As the load current decreasing, it smoothly switches to pulse frequency modulation (PFM) mode to keep high efficiency operation. ACM5620 provides accurate regulation over wide load and V_{IN} range and keeps low output ripple.

ACM5620 provides 22.8-V output overvoltage protection, cycle-by-cycle current limit protection and thermal shutdown protection.

ACM5620 is available in a 3.5-mm × 3.0-mm QFN package.

Device Information

Part number	Package	Body size (NOM)
ACM5620	QFN-FC-13	3.5 mm × 3.0 mm



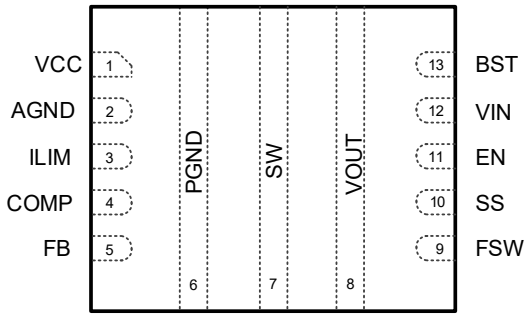
Typical Application Circuit

4. Device Comparison Table

Device	VIN Range /V	VOUT Range /V	Current Limit /A	R_{dson} /mΩ	Package
ACM5618	2.7 - 17.5	4.5 - 17.5	18	8/12	QFN-FC-13
ACM5620	2.7 - 20	4.5 - 21	20	6.5/10	QFN-FC-13

5. Pin Configuration and Function Descriptions

ACM5620
QFN-FC-13
3.5mm × 3.0mm



(Top View)

Pin No.	Name	I/O Type	Description
1	VCC	O	Output of the internal regulator. A ceramic capacitor of more than 1-μF is required between this pin and ground.
2	AGND	-	Analog signal ground of the IC. Connect the AGND to PGND via a single point on the printed circuit board. DO NOT connect the AGND to PGND underneath the IC.
3	ILIM	I	Programming the switching peak current limit by a resistor between this pin and AGND.
4	COMP	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and AGND.
5	FB	I	Output voltage feedback, a resistor divider connecting to this pin sets the output voltage.
6	PGND	-	Power ground.
7	SW	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power FET and the source of the internal high-side power FET.
8	VOUT	PWR	Boost converter output
9	FSW	I	The switching frequency is programmed by a resistor between this pin and the AGND. This pin can be left floating and the switching frequency will be set as default value.
10	SS	O	Soft-start programming pin. An external capacitor sets the ramp rate of the reference voltage of the internal error amplifier during soft start.
11	EN	I	Enable logic input. Logic high level enables the device and low level shut down the device.
12	VIN	I	IC power supply input.
13	BST	O	Power supply for high-side FET gate driver. A capacitor must be connected between this pin and the SW pin.

6. Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	BST	-0.3	SW + 6	V
Voltage	VIN, VOUT, SW, EN	-0.3	25	V
Voltage	ILIM, FB	-0.3	3.6	V
Voltage	Other pins	-0.3	6	V
T_A	Ambient operating temperature	-40	85	℃
T_{stg}	Storage temperature	-40	125	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicted under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001	±2000	V
		Charged-device model (CDM),per JEDEC specification JESD22-C101	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		20	V
VOUT	Output voltage range	4.5		21	V
L	Inductance (effective value)	0.47	2.2	10	μH
C_{IN}	Total input capacitance (effective value)	10			μF
C_{OUT}	Total output capacitance (effective value)	10	47	1000	μF
T_J	Junction Operating Temperature	-40		150	℃
T_A	Ambient Operating Temperature	-40		85	℃

6.4 Thermal Information

THERMAL METRIC		ACM5620 QFN-FC 13 PINS JEDEC STANDARD 4-LAYER PCB	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	60.2	℃/W
θ_{JT}	Junction-to-case (top) thermal resistance	28.6	℃/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	℃/W

6.5 Electrical Characteristics

Free-are room temperature 25℃, test conditions is V_{IN} = 3.7V, V_{OUT} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input voltage range		2.7		20	V
V_{IN_UVLO}	V_{IN} Undervoltage lockout (UVLO) threshold	V_{IN} Falling		2.4	2.6	V
V_{IN_HYS}	V_{IN} UVLO hysteresis			0.2		V
V_{CC_UVLO}	V_{CC} UVLO threshold	V_{CC} Falling		2.1		V
I_{Q_IN}	Quiescent current into V_{IN} pin	IC enabled, V_{EN} = 2V, no switching, V_{OUT} > 1.05 V_{IN} , V_{FB} = 1.1V			10	μA
I_{Q_OUT}	Quiescent current into V_{OUT} pin	IC enabled, V_{EN} = 2V, no switching, V_{OUT} > 1.05 V_{IN}, V_{FB} = 1.1V			200	μA
I_{SD}	Shutdown current	IC enabled, V_{EN} = 0V, no load, no feedback resistors. Measure the current into V_{IN} pin.		1	3	μA
V_{CC}	Internal regulator output voltage	I_{VCC} = 5mA, V_{IN} = 8V		5		V
EN INPUT						
V_{ENH}	EN high threshold voltage	V_{CC} = 5V			1.2	V
V_{ENL}	EN low threshold voltage	V_{CC} = 5V	0.4			V
R_{EN}	EN internal pull-down resistance	V_{CC} = 5V		800		kΩ
OUTPUT						
V_{OUT}	Output voltage range		4.5		21	V
I_{LKG_FB}	FB pin leakage current	V_{FB} = 1V			100	nA
I_{SS}	Soft-start charging current			5		μA
Power MOSFET						
$R_{DS(ON)}$	Low-side MOSFET ON-resistance	V_{CC} = 5V		6.5		mΩ
	High-side MOSFET ON-resistance	V_{CC} = 5V		10		
ERROR AMPLIFIER						
V_{REF}	Internal reference voltage on FB pin	Operating in PWM	0.985	1.000	1.015	V
		Operating in PFM		1.007		
I_{SOURCE}	Comp pin maximum sourcing current	V_{FB} = V_{REF} - 200mV, V_{COMP} = 1.5V		20		μA
I_{SINK}	Comp pin maximum sinking current	V_{FB} = V_{REF} + 200mV, V_{COMP} = 1.5V		20		μA
V_{COMPH}	COMP clamp voltage high	V_{FB} = V_{REF} - 200mV		2		V
V_{COMPL}	COMP clamp voltage low	V_{FB} = V_{REF} + 200mV		1		V
G_{EA}	Error amplifier trans-conductance			175		μA/V
G_{PS}	Power stage trans-conductance (ΔI_{L_PEAK} / ΔV_{COMP})			13.5		A/V
SWITCHING TIMING						
F_{SW}	Switching frequency	R_{FREQ} = 100 kΩ		550		kHz
T_{ON_MIN}	Low side Power FET minimum ON time	R_{FREQ} = 100 kΩ		70		ns
PROTECTION						
I_{LIM}	Peak current limit on power FET	R_{ILIM} = 91 kΩ	17.5	19.2		A
V_{OVP_THES}	V_{OUT} over-voltage protection threshold	V_{OUT} rising		22.8		V
V_{OVP_HYS}	V_{OUT} over-voltage protection auto-recovery hysteresis	V_{OUT} falling below V_{OVP_THES}		1.2		V
T_{OTSD}	Over-temperature shutdown threshold	T_J rising		160		℃
T_{OTSD_HYS}	Over-temperature shutdown auto-recovery hysteresis	T_J falling below T_{OTSD}		20		℃

6.6 Typical Characteristics

Test Condition: L=2.2μH, F_{SW}=550kHz, R_{ILIM}=110kΩ, Output capacitor 22μF MLCC×4 + 220μF E-cap.

Free-air room temperature 25℃ (unless otherwise noted)

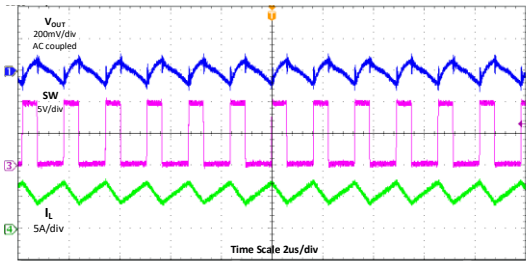


Figure 6-1 Switching Waveforms in CCM

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 2A)

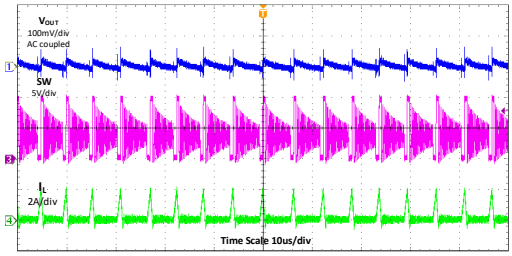


Figure 6-2 Switching Waveforms in PSM

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 50mA)

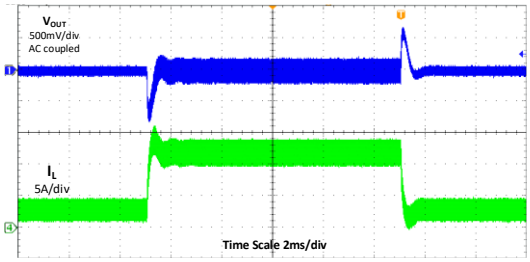


Figure 6-3 Load Transient

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 1 to 4A, 1A/μs)

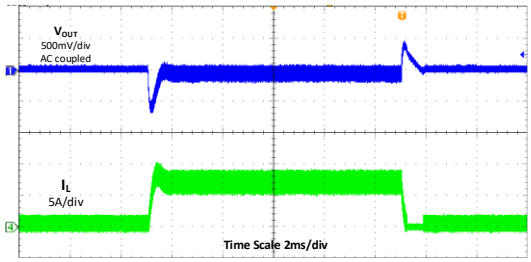


Figure 6-4 Load Transient

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 0.1 to 2.5A, 1A/μs)

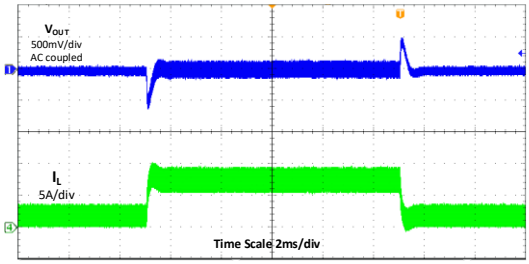


Figure 6-5 Load Transient

(V_{IN} = 10.8V, V_{OUT} = 19V, I_{OUT} = 1 to 4A, 1A/μs)

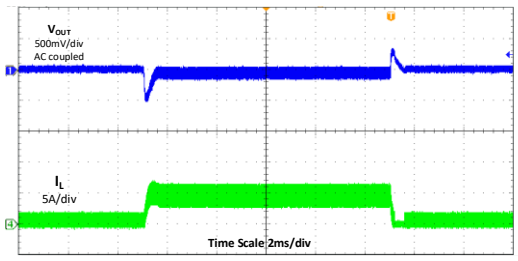


Figure 6-6 Load Transient

(V_{IN} = 10.8V, V_{OUT} = 19V, I_{OUT} = 0.1 to 2.5A, 1A/μs)

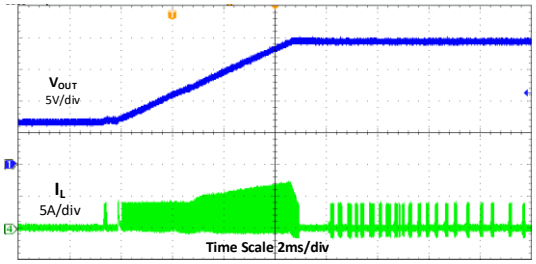


Figure 6-7 Soft start

(V_{IN} = 7.2V, V_{OUT} = 19V, C_{SS}=47nF, no load)

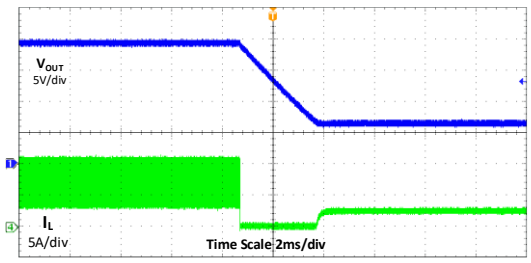


Figure 6-8 Power down

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 1A)

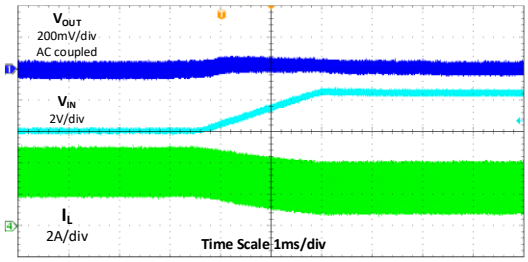


Figure 6-9 Line Regulation

(I_{OUT} = 1A, V_{OUT} = 19V, V_{IN} = 6 to 8.4V)

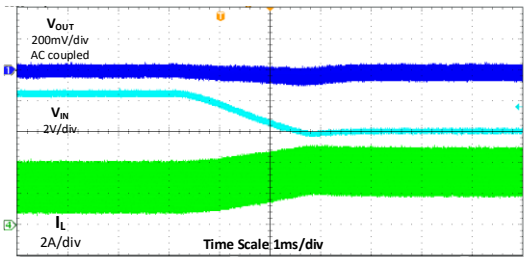


Figure 6-10 Line Regulation

(I_{OUT} = 1A, V_{OUT} = 19V, V_{IN} = 8.4 to 6V)

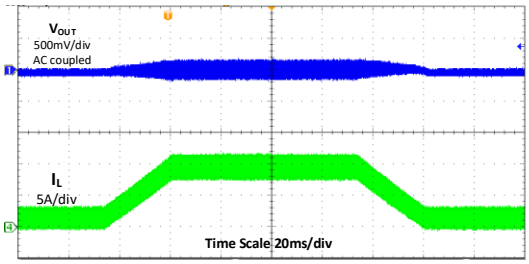


Figure 6-11 Load Sweep

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 0.5 to 4A)

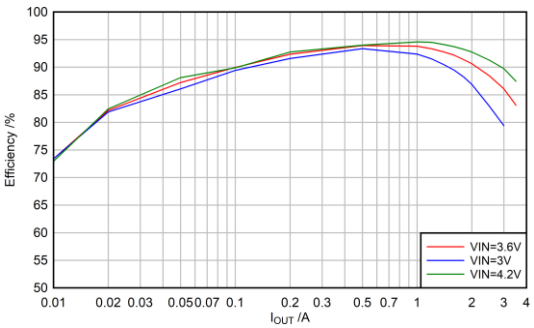


Figure 6-12Efficiency (1-s Li⁺ battery)

(V_{OUT} = 19V, I_{OUT} = 0~3A, F_{SW}=300kHz)

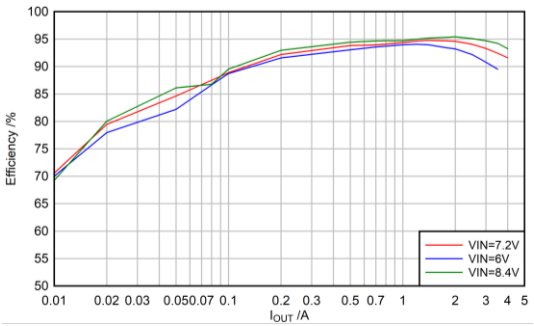


Figure 6-13 Efficiency (2-s Li⁺ battery)

(V_{OUT} = 19V, I_{OUT} = 0~4A, F_{SW}=300kHz)

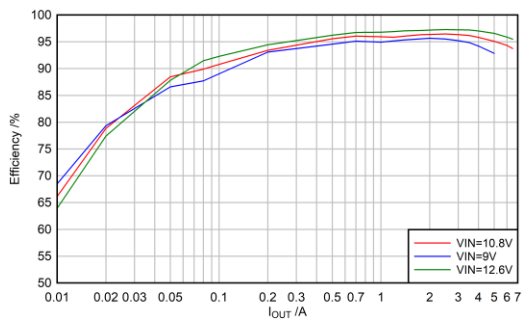


Figure 6-14 Efficiency (3-s Li⁺ battery)

(V_{OUT} = 19V, I_{OUT} = 0~6A, F_{SW}=300kHz)

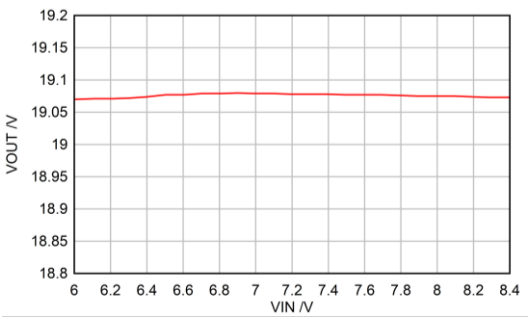


Figure 6-15 Line Regulation

(V_{OUT} = 19V, I_{OUT} = 1A)

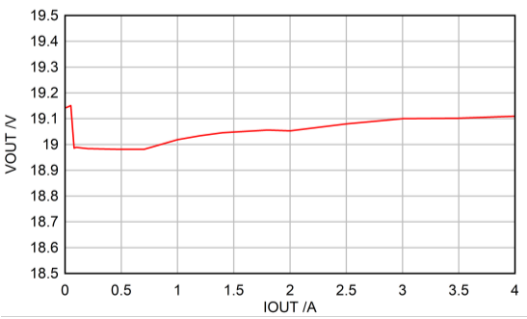


Figure 6-16 Load Regulation

(V_{IN} = 7.2V, V_{OUT} = 19V, I_{OUT} = 0~4A)

7. Detailed Description

7.1 Overview

The ACM5620 is a fully-integrated synchronous boost converter with an 6.5-mΩ power switch and a 10-mΩ rectifier switch to deliver high power from a 2-s cell or 3-s cell Lithium batteries. The input voltage range is 2.7-V to 20-V and the output range is 4.5-V to 21-V.

The ACM5620 employs adaptive constant off-time peak current control mode to regulate the output voltage. In moderate-to-heavy load condition, the ACM5620 works in the quasi-constant frequency pulse width modulation (PWM) mode. The switching frequency in PWM mode is adjustable among 300kHz/550kHz/800kHz/1MHz by an external resistor. In light load condition, the ACM5620 works in pulse frequency modulation (PFM) mode, which skips the unnecessary pulses and keeps high efficiency. The ACM5620 implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The switch peak current limit is programmable by an external resistor. The ACM5620 uses external loop compensation, which provides flexibility to use different inductors and output capacitors. The adaptive off-time peak current control scheme gives excellent line/load transient response with minimal output capacitance.

7.2 Functional Block Diagram

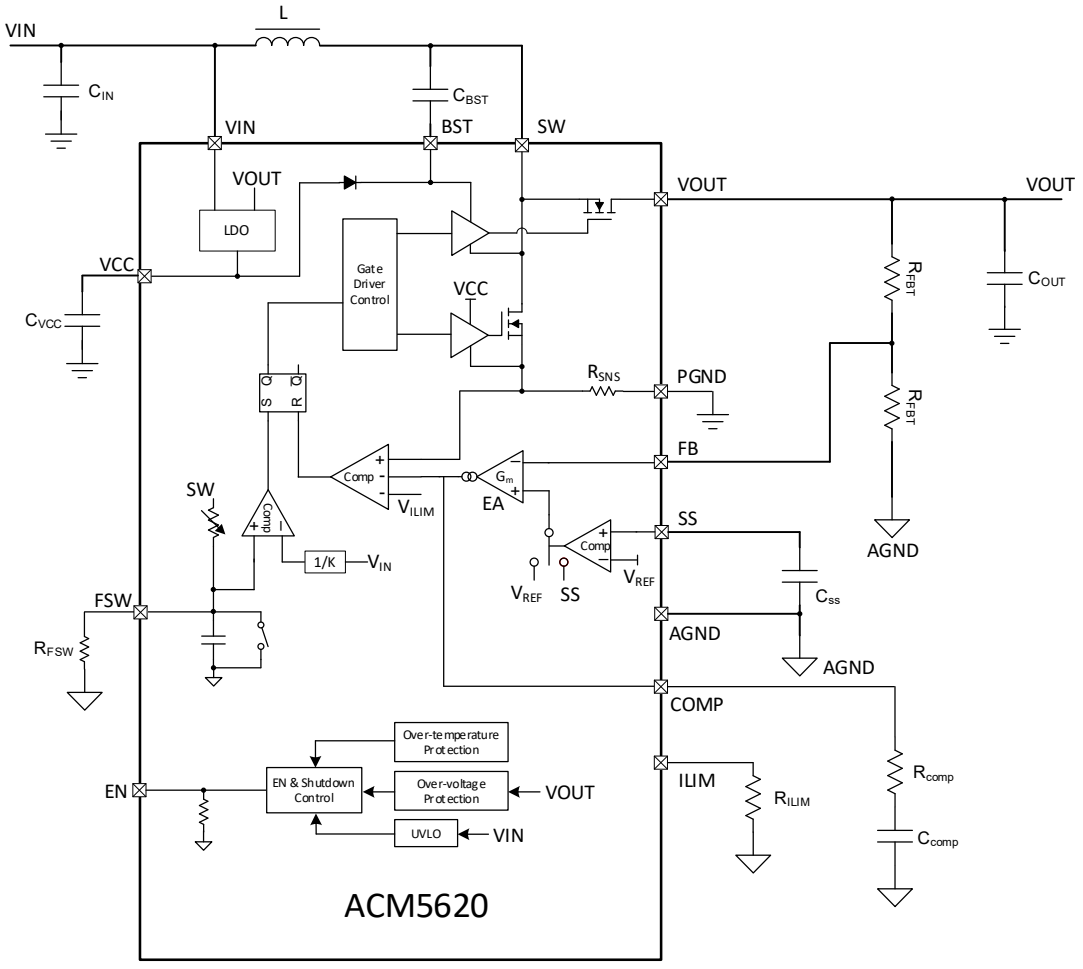


Figure 6-1. Functional Block Diagram

7.3 Detail Feature Description

6.3.1 Enable and Start-up

The ACM5620 has an EN pin to enable or disable the device. Pulling the EN pin to logic high, the device is enabled and the start-up sequence is initialized. Pulling the EN pin to logic low, the device is disabled. The switching is stopped and the output starts to decay.

During the start-up, the ACM5620 supports adjustable soft-start function to avoid in-rush current. The device sources a constant current of 5-μA typically out of the SS pin, charging the external capacitor C_{ss} and building a ramping up voltage. This voltage is fed into the positive input of the internal error amplifier until it goes higher than the internal reference voltage, which is 1-V typically. The capacitance connected to the SS pin determines how fast the VOUT ramps up. Equation 6-1 gives the calculation of the soft-start time,

$$t_{ss} = \frac{V_{REF} \times C_{SS}}{I_{SS}} \qquad \text{(Eq.6-1)}$$

where,

- t_{ss} is the soft-start time
- V_{REF} is the internal reference voltage, which is 1-V typically
- C_{SS} is the external capacitance connected to SS pin
- I_{SS} is the soft-start charging current, which is 5-uA typically

A 47-nF capacitor could cover most application circumstances. As the SS voltage ramps up during the soft-start phase, once it exceeds the internal reference voltage, the positive input of the internal error amplifier is taken over by the internal reference voltage, indicating the soft-start phase is completed. When the EN pin is pulled low, the C_{ss} is discharged to GND.

6.3.2 Undervoltage Lockout

The UVLO feature protects the device from the possible malfunction when operating at low input voltage, which could result from an excessively discharged battery or a brownout event. The ACM5620 monitors both the VIN and VCC for the UVLO. When the VIN falling below the UVLO threshold V_{IN_UVLO}, which is typically 2.6-V, the ACM5620 stops switching. The ACM5620 will not recover to operate until VCC and VIN get higher than (V_{IN_UVLO} +200mV). When the VCC falling below the UVLO threshold V_{CC_UVLO}, which is typically 2.4-V, the ACM5620 stops switching.

6.3.3 Adjustable Switching Frequency

The ACM5620 provide four options of switching frequency. Low switching frequency provides higher efficiency but may not have good transient performance. It should also be noted that higher switching frequency results in lower inductor current ripple, which may be the bottle-neck in some high VOUT/VIN ratio applications. ACM5620 employs an external resistor R_{FSW} connected between FSW pin and GND to set the switching frequency. If the FSW pin is left floating, the switching frequency will be set to 550-kHz as default. Table 6-1 shows the detail configurations.

Table 6-1. Switching Frequency Options

R_{FSW}	Switching Frequency
51 kΩ	300 kHz
100 kΩ or floating	550 kHz
200 kΩ	800 kHz
390 kΩ	1 MHz

6.3.4 Adjustable Peak Current Limit

To avoid excessive peak current on power switch, an internal cycle-by-cycle current limit is implemented on ACM5620. In battery powered systems, the adjustable peak current limit could also be used to limit the battery discharge current to avoid brownout events. The low-side switch will be turned off immediately once the current arrives the current limit. The peak switch current limit can be programmed by an external resistor connected between ILIM pin and GND. Use Equation 6-2 to calculate the resistor value for a selected current limit,

$$I_{LIM} = \frac{1750}{R_{ILIM}} \qquad \text{(E.q. 6-2)}$$

where,

- R_{ILIM} (kΩ) is the resistance connected between ILIM pin and GND
- I_{LIM} (A)is the switch peak current limit

6.3.5 Overvoltage Protection

The ACM5620 stops switching immediately when the VOUT exceeds the output overvoltage protection threshold V_{OVP_THES}, which is 22-V typically. The normal operation will not recover until the VOUT drops a hysteresis value lower than the V_{OVP_THES}, which is typically 1.5-V. The over voltage protection is non-latched and the device could automatically recover after the fault condition removed.

6.3.6 Over Temperature Protection

An over-temperature protection is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown is triggered when the junction temperature exceeds 160°C. The normal operation will not recover until the junction temperature falls below 130°C typically. The over temperature protection is non-latched and the device could automatically recover after the fault condition removed.

6.4 Device Function Modes

6.4.1 Operation

6.4.1.1 PWM Mode

The synchronous boost converter ACM5620 employs adaptive-off time control scheme. It operates at a quasi-constant frequency pulse width modulation in moderate-to-heavy load condition. The ACM5620 integrates a dedicate circuit to predict the low-side off-time based on the VIN and VOUT voltage. At the beginning of each period, the low-side switch is turned on. The inductor current starts to ramp up. The low-side current is sensed and compared to the output of the error amplifier. Once the comparator output toggled, the low-side switch is turned off and the inductor current starts to ramp down. After a dead-time duration, the high-side switch is turned on, taking over the inductor current from its body diode. The high-side switch keeps ON status until the time-out event from the off-time prediction circuit. Then the low-side switch turns on after a dead time duration and a new period starts.

6.4.1.2 PFM Mode

At light load conditions, the ACM5620 automatically enters the pulse frequency modulation (PFM) mode. As the loading current goes down, the current flowing through the high-side switch decreases to zero during the off time. The high side switch is turned

off at zero-crossing point. The status is kept until next period starts and the low side switch turned on. If the loading current continuously decrease and reaches a threshold of 1/12 I_{LIM}, the output of the error amplifier is clamped at this value. If the loading current is still lower than the average current ACM5620 delivers, the output voltage increases above the nominal setting output voltage. The ACM5620 extends the off-time to decrease the energy delivered to the output and regulate the output voltage to 0.8% higher than the nominal setting.

7 Application and Implementation

7.1 Application Information

The ACM5620 is capable to support up to 21-V output voltage and up to 20-A switch current, delivering over 80-W output power from 2-s battery, or 120W from 3-s battery. It is quite suitable for applications powered by 2-s cell and 3-s cell Li^+ battery. The ACM5620 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate-to-heavy load condition. In light load condition, the ACM5620 operates in PFM mode, keeping high efficiency in entire loading range. The ACM5620 employs the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The ACM5620 works well with various inductor and output capacitor combinations by external loop compensation. It also supports four switching frequency options and programmable current limit.

7.2 Typical Application

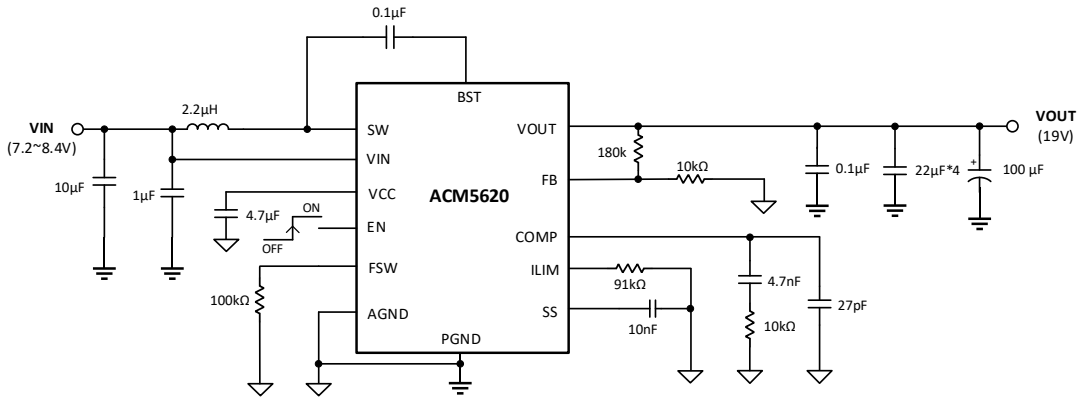


Figure 7-1 ACM5620 7.4V to 19V/4A Application circuit

7.2.1 Design Requirements

Table 7-1. Design Parameters

Design Parameters	Recommended Values
Input voltage range	7.2~8.4V
Output voltage	19V
Output voltage ripple (V_{pp})	<100mV
Switching Frequency	550kHz
Current Limit	19A

7.2.2 Detailed Design Procedure

7.2.2.1 Switching Frequency Setting

The ACM5620 supports 4 switching frequency options. The switching frequency is set by the resistance connected between FSW pin and GND. In this example, a 100-kΩ resistor is connected to set the 550-kHz F_{sw} to take a balance among efficiency, thermal and line/load transient performance.

7.2.2.2 Peak Current Limit Setting

7.2.2.3 Output Voltage Setting

For ACM5620, the output voltage is set by an external resistor divider (R1, R2 in Figure 7-1). Typically, a minimum current of 30-μA flowing through the feedback divider gives good accuracy and noise rejection, thus a standard 33-kΩ resistor is selected for the bottom resistor in the divider. Equation 7-1 gives the output voltage setting calculation,

$$R_1 = \frac{(V_{OUT}-V_{REF})\times R_2}{V_{REF}} \qquad \text{(Eq. 7-1)}$$

7.2.2.4 Inductor Selection

As the inductor has significant impact on the steady state operation of the power supply, transient performance, loop stability and efficiency, the inductor is the most important component in switching power regulator design. Four main specifications for

the inductor selection are the inductance, the DC resistance, the saturation current and the rated DC current.

The ACM5620 is designed to work with 0.47-µH~10-µH inductance. A 0.47-µH inductor is typically available in a smaller or lower-profile package with higher saturation current and rated DC current capability, while a 10-µH inductor produces lower inductor current ripple. If the output current is limited by the peak current limit of the IC, using a 10-µH inductor can maximize the output current capability of the boost converter.

Usually, the inductance can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, the inductance can decrease 20% to 30% from nominal value, depending on how the inductor vendor defines saturation current. When selecting an inductor, make sure the saturation current is higher than its peak current during the operation and the rated DC current is higher than the RMS value of the inductor current in normal operation.

Follow Equation 7-3 and Equation 7-4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, it is recommended to use the minimum switching frequency, the inductor value with 30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 7-2.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \qquad \text{(E.q. 7-2)}$$

where,

- V_{OUT} is the output voltage
- I_{OUT} is the output current
- V_{IN} is the input voltage
- η is the efficiency of the boost circuit

Inductor current ripple is given by Equation 7-3,

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times F_{SW}} \qquad \text{(E.q. 7-3)}$$

where,

- I_{PP} is the peak-to-peak current ripple on the inductor
- L is the inductor value
- F_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Furthermore, the peak current, I_{L_PEAK} is given by,

$$I_{L_{peak}} = I_{DC} + \frac{I_{PP}}{2} \qquad \text{(E.q. 7-4)}$$

The current limit of the ACM5620 should be set higher than the peak current I_{L_peak}. The saturation current of the inductor should be higher than the current limit setting.

Boost converter efficiency mainly depends on the resistance of the current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The ACM5620 has optimized the internal switch resistance. However, the overall efficiency is still affected significantly by the DC resistance (DCR) of the inductor and the inductor core loss. The core loss is related to the magnetic material of the core. Different inductors could have quite different core loss performance. Larger inductor current ripple generates higher DCR conduction losses and higher core loss. In most cases, the core loss information is not shown on the inductor datasheet. If needed, consult the inductor vendor for detailed information. Generally, ACME would recommend an inductor with lower DCR. However, there is always tradeoff among the inductance, DCR and its footprint.

7.2.2.5 Input Capacitor Selection

For battery powered systems, to smooth the battery discharge current, large input capacitance is recommended, for example, a 220-μF electrolytic capacitor. For other none battery powered systems, usually a 22-μF capacitance is good enough. As a rule of thumb, a sufficient input capacitance should make the input voltage ripple lower than 100-mV.

The VIN pin is the power supply for the ACM5620, a 0.1-μF low-ESR ceramic bypass capacitor is recommended and should be placed as close as possible to the VIN pin. The VCC is the output of the internal LDO. Connect a 1-μF ceramic capacitor between VCC pin and AGND is recommended for normal operation of the internal LDO.

It should also be noted that the effective capacitance of the ceramic capacitors may decrease as the DC voltage across the capacitor increase, which is also known as DC bias effect. Make sure there is enough effective capacitance for all the capacitors mentioned above.

7.2.2.6 Output Capacitor Selection

For the applications where lower output voltage ripple is the priority, ACME recommends low-ESR output capacitors like MLCC. Typically, three 22-μF ceramic output capacitors works well for most applications. Take care when evaluating the derating of a capacitor under DC bias. The bias can significantly reduce effective capacitance of the MLCC. Ceramic capacitors may lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating is necessary to ensure adequate effective capacitance.

For the applications where good load transient performance is required, a larger output capacitance is recommended. Electrolytic capacitors and MLCC can be put in parallel to balance the output ripple and stable output during load transient events. However, in some applications where the boost output voltage dynamically changes, for example, the Class-H application with ACME audio amplifiers, large output capacitance may increase the burden of the input current peak, as it takes extra current to charge the output capacitance up and raise the output voltage.

Use the Equation 7-5 to Equation 7-7 to estimate the output capacitance according to the output ripple requirement.

$$V_{ripple\_cap} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times F_{SW} \times C_{OUT}} \quad \text{(E.q. 7-5)}$$

$$V_{ripple\_res} = I_{L\_peak} \times R_{C\_ESR} \quad \text{(E.q. 7-6)}$$

$$V_{ripple} = \sqrt{V_{ripple\_cap}^2 + V_{ripple\_res}^2} \quad \text{(E.q. 7-7)}$$

where,

- V_{ripple_cap} is output voltage ripple caused by charging and discharging of the output capacitor
- V_{ripple_res} is output voltage ripple caused by ESR of the output capacitor
- V_{IN_MIN} is the minimum input voltage of boost converter
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- I_{L_peak} is the peak current of the inductor
- F_{SW} is the converter switching frequency
- R_{C_ESR} is the ESR of the output capacitors

7.2.2.7 Loop Stability

The ACM5620 requires external loop compensation, which usually formed by a serial R-C network connected to COMP pin. The COMP pin is the output of the internal error amplifier. A capacitor can also be added in parallel with the serial R-C to provide extra high frequency rolling. The detail calculation steps for loop compensation design will be discussed in the following section.

The small-signal model transfer function of power stage is given by Equation 7-8,

$$G_{PS}(s) = \frac{R_O \times (1-D)}{2 \times R_{SNS}} \times \frac{(1-\frac{s}{2\pi \times f_{RHPZ}})(1+\frac{s}{2\pi \times f_{ESRZ}})}{(1+\frac{s}{2\pi \times f_p})} \quad \text{(E.q. 7-8)}$$

where,

- D is the switching duty cycle
- R_O is the output load resistance
- R_{SNS} is the equivalent internal current sense resistor, which is 0.0075 Ω

The f_{RHPZ} is the right half plane zero, given by

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \quad \text{(E.q. 7-9)}$$

where,

- L is the inductance

The f_{ESRZ} is the zero introduced by the equivalent series resistance of the output capacitor, given by

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad \text{(E.q. 7-10)}$$

The f_p is the dominant load pole, given by,

$$f_p = \frac{2}{2\pi \times R_O \times C_{OUT}} \quad \text{(E.q. 7-11)}$$

The COMP pin is connected to the output of the internal error amplifier, which is a trans-conductance amplifier. The overall transfer function of the feedback and compensation blocks is given by,

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1+\frac{s}{2\pi \times f_{z\_COMP}})}{(1+\frac{s}{2\pi \times f_{p\_COMP}})(1+\frac{s}{2\pi \times f_{p\_ROLL}})} \quad \text{(E.q. 7-12)}$$

where

- G_{EA} is the transconductance of the amplifier
- R_{EA} is the output resistance of the amplifier
- V_{REF} is the reference voltage on the FB pin
- V_{OUT} is the output voltage

The f_{p_COMP}, f_{p_ROLL} are the poles introduced by the compensation network, given by

$$f_{p\_COMP} = \frac{1}{2\pi \times R_{EA} \times C_{COMP}} \quad \text{(E.q. 7-13)}$$

where

- R_{EA} is the equivalent output resistance of the error amplifier
- C_{COMP} is the capacitor in the R-C compensation network

$$f_{p\_ROLL} = \frac{1}{2\pi \times R_{COMP} \times C_{ROLL}} \quad \text{(E.q. 7-14)}$$

where

- R_{COMP} is the resistor in the R-C compensation network
- C_{ROLL} is the optional capacitor in parallel with the R-C compensation network

The f_{z_COMP} is the zero introduced by the compensation network, given by,

$$f_{z\_COMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad \text{(E.q. 7-15)}$$

8. Layout

Note:

A. All the pins which referred to AGND, including VCC, FSW, FB, COMP, SS, ILIM should be tied to AGND. The AGND(pin 2) and PGND(pin 6) should be tied together at a single point.

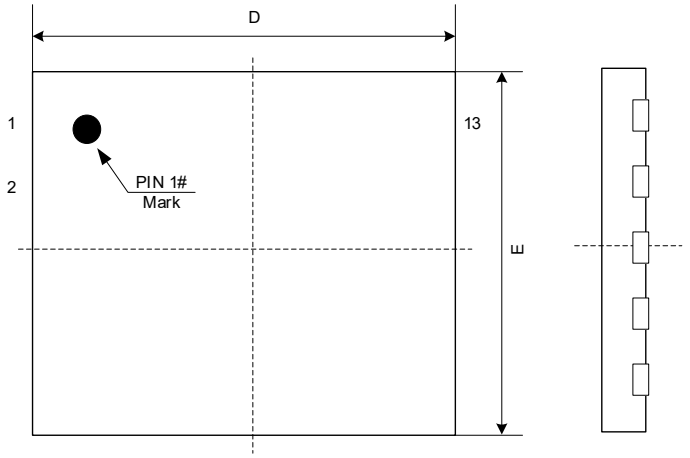
B. DO NOT connect the AGND and PGND together under the IC. Place a cut-out area to make sure the AGND is not tied to PGND by automatic polygon pour.

C. Place the 0.1μF or 1μF COUT as close as possible to the VOUT and PGND pin, and minimize the loop area of VOUT-COUT-PGND.

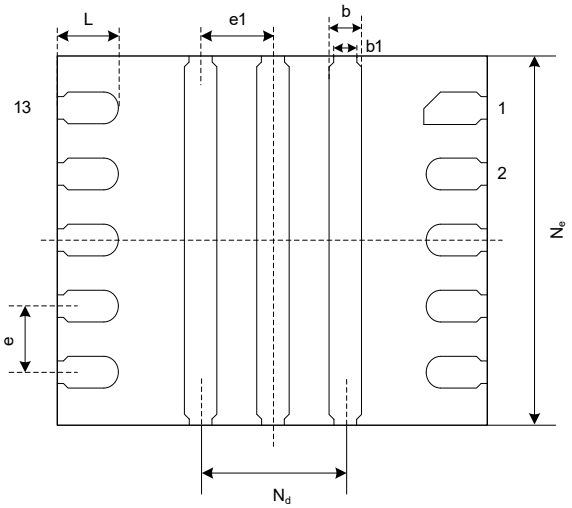
D. Vias could be placed near the IC to help power dissipation.

9. Package Dimensions

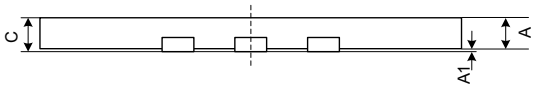
TOP VIEW



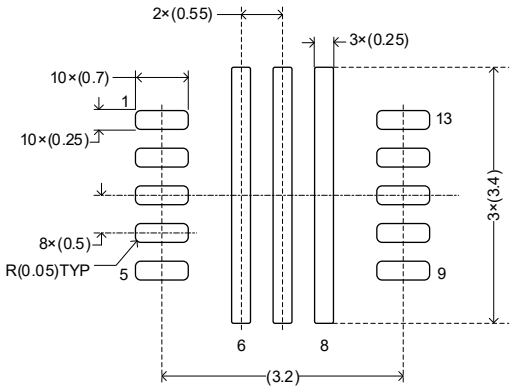
BOTTOM VIEW



SIDE VIEW



Symbol	Dimension (mm)		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c		0.203 REF	
D	3.40	3.50	3.60
e		0.50 BSC	
e1		0.55 BSC	
Nd		1.10 BSC	
E	2.90	3.00	3.10
Ne		2.00 BSC	
L	0.45	0.50	0.55
h	0.10	0.15	0.20



RECOMMENDED LAND PATTERN

10. Order Information

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM5620	QFN-FC-13 Tape and Reel	5000	5000	RoHS Compliant Lead-Free Finish	MSL3	ACM5620