

5.5 V, 6 A/8 A/10 A, 1.2 MHz, High-Efficiency, Synchronous Step-Down Converter

■ Features

- Low $R_{DS(ON)}$ for internal switches (Top / Bottom): 8 / 8 m Ω
- Operating input range: 2.4 V to 5.5 V
- Quiescent current: 15 μ A
- Switching frequency: 1.2 MHz
- Adjustable output from 0.6 V to V_{IN}
- Fixed output from 0.4 V to 1.6 V
- Up to 10 A output capability
 - DIO6146X06: 6 A output current
 - DIO6146X08: 8 A output current
 - DIO6146X10: 10 A output current
- Adjustable soft start
- Output discharge resistance: about 5 Ω
- 100% duty cycle in dropout
- 1% feedback accuracy
- External mode control
 - A: Hiccup mode
 - B: Latching mode
- Stable with low-ESR output ceramic capacitors
- Thermal shutdown

■ Applications

- Mobile or battery-powered devices
- IP network cameras
- Machine vision cameras
- Storage (SSD, HDD)

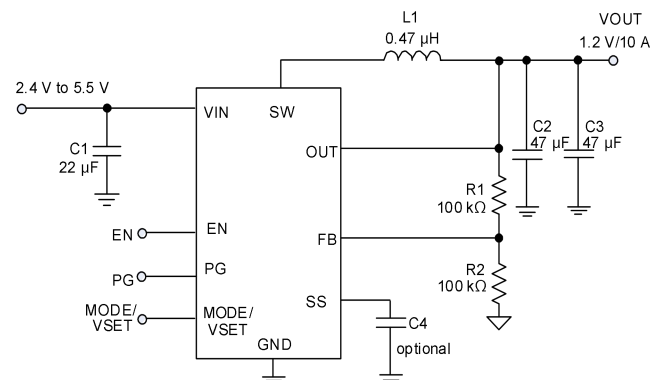
■ Package Information

Part Number	Package	Body Size
DIO6146	QFN-12	2 mm × 3 mm

■ Description

The DIO6146 is a step-down DC-DC converter with power MOSFETs integrated. It is able to provide a continuous output current of up to 10 A. The output voltage can be regulated as low as 0.4 V. It also offers various protection schemes such as current-limit and thermal shutdown. Optimized COT architecture (Constant On-Time) allows both fast transient response and loop stability. Housed in a small flip-chip based QFN2*3-12 package, the DIO6146 requires minimal external components to implement up to 10 A output capability with superior thermal performance.

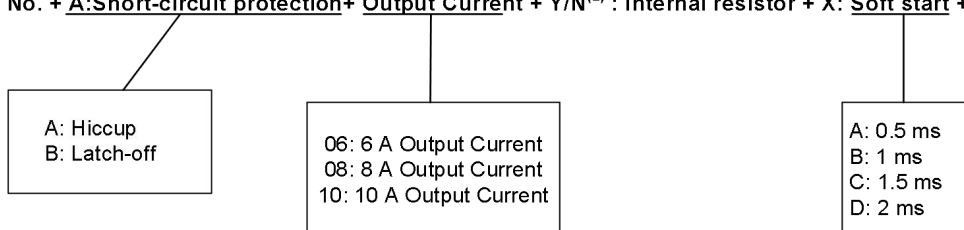
■ Simplified Schematic



■ Ordering Information

Ordering Part No.	Top Marking ⁽¹⁾	MSL	RoHS	T _J	Package	
DIO6146A06YXQN12	FAFYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146A06NXQN12	FAFNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146A08YXQN12	FAHYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146A08NXQN12	FAHNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146A10YXQN12	FAKYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146A10NXQN12	FAKNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B06YXQN12	FBFYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B06NXQN12	FBFNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B08YXQN12	FBHYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B08NXQN12	FBHNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B10YXQN12	FBKYX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000
DIO6146B10NXQN12	FBKNX	3	Green	-40°C to 125°C	QFN2*3-12	Tape & Reel, 3000

Ordering Number = Part No. + A:Short-circuit protection + Output Current + Y/N⁽²⁾ : Internal resistor + X: Soft start + Package code



Note:

- (1) The "X" in Top Marking represents the soft-start code. 0.5 ms: A; 1 ms: B; 1.5 ms: C; 2 ms: D.
 (2) Y: Built-in pull-up resistor; N: No built-in resistor; If Y, then connect PG to VIN, EN to GND, and VSET to GND.

Part Number	Output Voltage Range	Start-up Voltage	Version	Output Current
DIO6146A06	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Hiccup	6 A
DIO6146A08	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Hiccup	8 A
DIO6146A10	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Hiccup	10 A
DIO6146B06	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Latch-off	6 A
DIO6146B08	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Latch-off	8 A
DIO6146B10	0.4 V to V _{IN}	Adjustable or fixed (selectable by external resistor on VSET/MODE)	Latch-off	10 A

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

List of Contents

1. Pin Assignment and Functions	1
2. Absolute Maximum Ratings	2
3. Recommended Operating Conditions	2
4. ESD Ratings	3
5. Electrical Characteristics	4
6. Typical Characteristics	6
7. Block Diagram	9
8. Function Description	10
8.1. Overview	10
8.2. FPWM	10
8.3. PSM	10
8.4. 100% duty	10
8.5. Soft start	11
8.6. Short-circuit protection	11
8.7. Undervoltage lockout (UVLO)	12
8.8. Thermal shutdown (TSD)	12
8.9. Device functional modes	12
9. Application Information	15
9.1. Typical application	15
10. Physical Dimensions: QFN2*3-12	17

List of Figures

Figure 1. QFN2*3-12 (Top view)	1
Figure 2. Efficiency	6
Figure 3. Load regulation	6
Figure 4. Power on	6
Figure 5. Power on	6
Figure 6. EN on	6
Figure 7. EN on	6
Figure 8. Output voltage ripple	7
Figure 9. Output voltage ripple	7
Figure 10. Output voltage ripple	7
Figure 11. Load transient	7
Figure 12. Load transient	7
Figure 13. Load transient	7
Figure 14. Hiccup short-circuit protection	8
Figure 15. Hiccup short-circuit protection	8
Figure 16. Soft-start sequence	11
Figure 17. Typical application circuit (DIO6146X06)	15
Figure 18. Typical application circuit (DIO6146X10)	15

List of Tables

Table 1. PG function	13
Table 2. Voltage selection	13
Table 3. Design parameters	16
Table 4. List of components	16

1. Pin Assignment and Functions

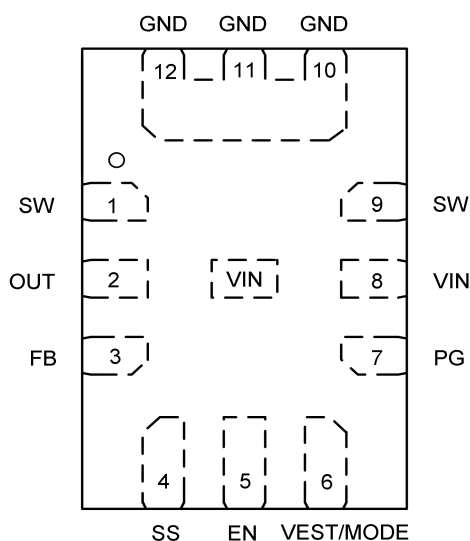


Figure 1. QFN2*3-12 (Top view)

Pin Name	Type	Description
SW	P	Switch pin of the power stage.
OUT	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
FB	I	Voltage feedback input. Connect the output voltage resistor divider to this pin. When using a fixed output voltage, connect directly to OUT.
SS	I	Soft-start pin. An external capacitor can adjust the soft-start time. If unused, leave this pin floating to set a default SS time.
EN	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
VEST /MODE	I	Connecting a resistor to GND selects one of the fixed output voltages. Tying the pin high or low selects an adjustable output voltage. After the device has started up, the pin operates as a MODE input. Applying a high level selects forced PWM mode operation and a low level selects power-save mode operation.
PG	O	Power-good open-drain output pin. The pull-up resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
VIN	P	Power supply input voltage pin.
GND		Power ground pin.

Note:

(1) I = input, O = output, P = power.

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
Voltage	VIN, EN, OUT, FB, PG, VSET/MODE, SS voltage	-0.3 to 6	V
	SW (DC)	-0.3 to VIN + 0.3	
	SW (AC, less than 10 ns) ⁽²⁾	-2.5 to 10	
ISINK_PG	Sink current at PG	1	mA
TJ	Junction temperature	-40 to 150	°C
TSTG	Storage temperature	-65 to 150	°C

Note:

(1) All voltage values are with respect to network ground terminal.

(2) While switching.

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Rating	Unit
VIN	Supply voltage range		2.4 to 5.5	V
VOU	Output voltage range		0.4 to VIN	V
VIN_SR	Falling transition time at VIN ⁽¹⁾		10	mV/μs
IOUT	Output current	DIO6146X06	6	A
		DIO6146X08	8	A
		DIO6146X10	10	A
TJ	Junction temperature		-40 to 125	°C

Note:

(1) The falling slew rate of VIN must be limited if VIN goes below VUVLO.

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
HBM	ANSI/ESDA/JEDEC JS-001	±4	kV
CDM	ANSI/ESDA/JEDEC JS-002	±2	kV

5. Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , and $V_{IN} = 2.4\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$, unless otherwise noted.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
Supply							
I _{Q_VIN}	Quiescent current		EN = High, no load, device not switching, T _J = 25°C		15	25	μA
I _{Q_OUT}	Operating quiescent current into OUT pin		EN = High, no load, device not switching, V _{OUT} = 1.8 V, T _J = 25°C		12		μA
I _{SD}	Shutdown current		EN = Low, T _J = 25°C		0.24	0.75	μA
V _{UVLO}	Undervoltage lockout threshold		V _{IN} rising	2.2	2.3	2.4	V
			V _{IN} falling	2.1	2.2	2.3	V
T _{SD} ⁽¹⁾	Thermal shutdown threshold		T _J rising		150		°C
T _{SD_HYS} ⁽¹⁾	Thermal shutdown hysteresis		T _J falling		20		°C
Logic interface EN, SDA, SCL							
V _{IH}	High-level input threshold voltage at EN, VSET/VID			0.9			V
V _{IL}	Low-level input threshold voltage at EN, VSET/VID					0.4	V
I _{EN,LKG}	Input leakage current into EN pin		T _J = 25°C		0.01	0.1	μA
Start-up, power good							
t _{Delay}	Enable delay time		Time from EN high to device starts switching, 249 kΩ resistor connected between VSET/MODE and GND	420	840	1200	μs
t _{Ramp}	Output voltage ramp time	DIO6146A06NC DIO6146B06NC	Time from device starts switching to power good (no external capacitor connected)	1	1.5	1.85	ms
		DIO6146A08NA DIO6146A10NA DIO6146B08NA DIO6146B10NA		0.4	0.55	0.72	ms
I _{SS}	SS pin source current				20		μA
t _{PG, DLY}	Power good deglitch delay		Rising and falling edges		34		μs
V _{PG}	Power good lower threshold		V _{OUT} referenced to V _{OUT} nominal	85	91	96	%
	Power good upper threshold		V _{OUT} referenced to V _{OUT} nominal	103	111	120	%
V _{PG,OL}	Low-level output voltage		I _{Sink} = 1 mA			0.36	V

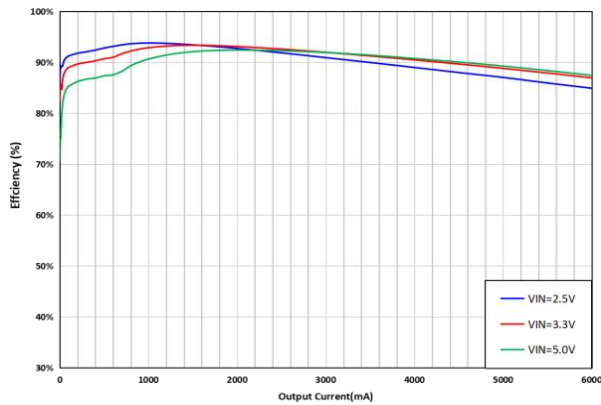
$I_{PG,LKG}$	Input leakage current into PG pin	$V_{PG} = 5.0\text{ V}$, $T_J = 25^\circ\text{C}$		0.01	0.1	μA
Output						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, $T_J = 25^\circ\text{C}$	-0.7		0.7	%
		Fixed voltage operation, FPWM, no load, $T_J = -40^\circ\text{C}$ to 125°C	-1		1	%
V_{FB}	Feedback voltage	Adjustable voltage operation $T_J = -40^\circ\text{C}$ to 125°C	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation $V_{FB} = 0.6\text{ V}$, $T_J = 25^\circ\text{C}$		0.01	0.1	μA
R_{DIS}	Output discharge resistor at OUT pin			4.3		Ω
	Load regulation	$V_{OUT} = 0.9\text{ V}$, FPWM		0.04		%/A
Power switch						
$R_{DS(ON)}$	High-side FET on-resistance			8		m Ω
	Low-side FET on-resistance			8		m Ω
$I_{LIM}^{(1)}$	High-side FET forward current limit	DO6146X06	7	9	11	A
		DO6146X08	10	12	14	A
		DO6146X10	12	14	16	A
	Low-side FET forward current limit	DO6146X06		6.5		A
		DO6146X08		9		A
		DO6146X10		12		A
	Low-side FET negative current limit	DO6146X06, DO6146X08, DO6146X10		-3		A
f_{SW}	FPWM switching frequency	$I_{OUT} = 1\text{ A}$, $V_{OUT} = 0.9\text{ V}$		1.2		MHz

Note:

- (1) Guaranteed by characterization.
(2) Specifications subject to change without notice.

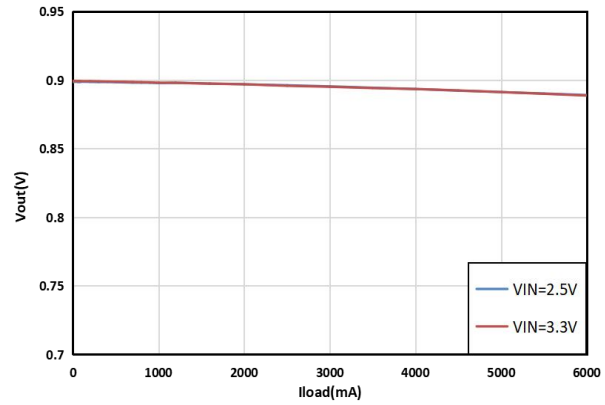
6. Typical Characteristics

$V_{IN} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.



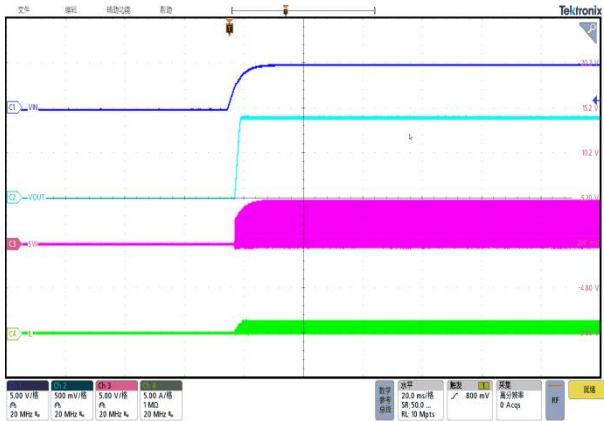
$V_{OUT} = 0.9\text{ V}$

Figure 2. Efficiency



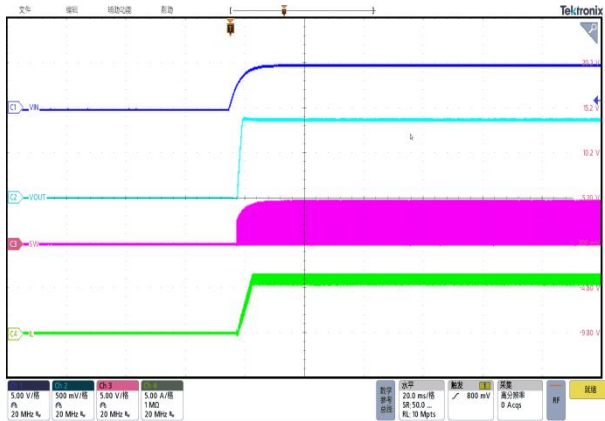
$V_{OUT} = 0.9\text{ V}$

Figure 3. Load regulation



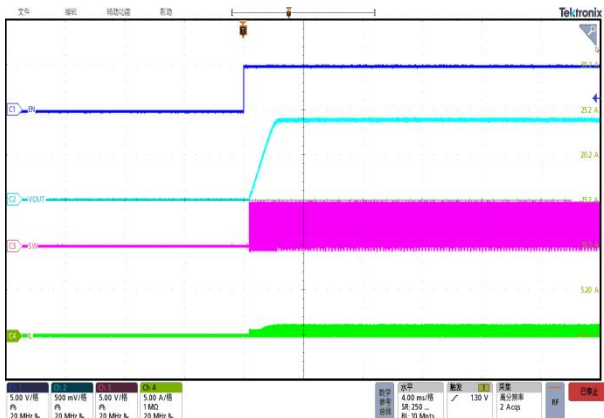
$I_{OUT} = 0.01\text{ A}$, PSM operation

Figure 4. Power on



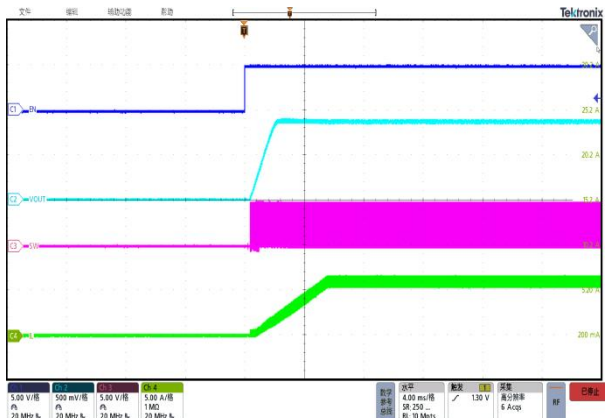
$I_{OUT} = 6\text{ A}$, PSM operation

Figure 5. Power on



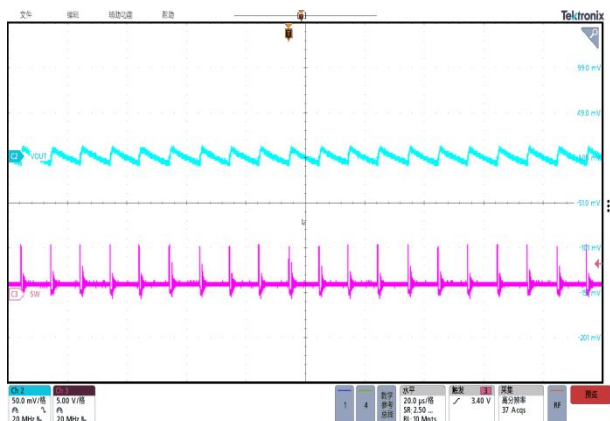
$I_{OUT} = 0.01\text{ A}$, PSM operation

Figure 6. EN on



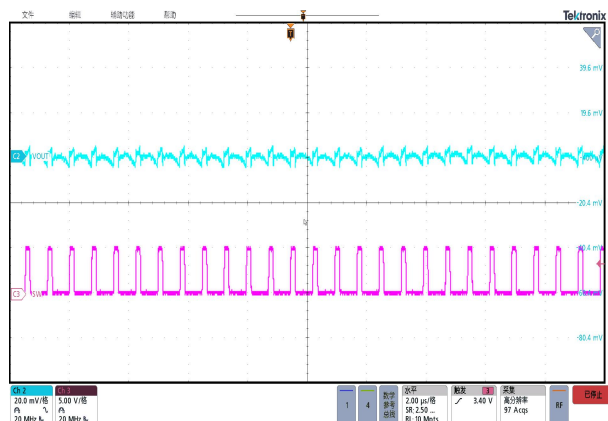
$I_{OUT} = 6\text{ A}$, PSM operation

Figure 7. EN on



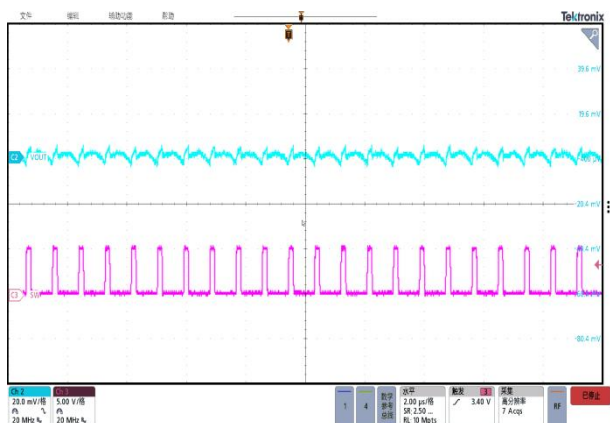
$I_{OUT} = 0.05\text{ A}$, PSM operation

Figure 8. Output voltage ripple



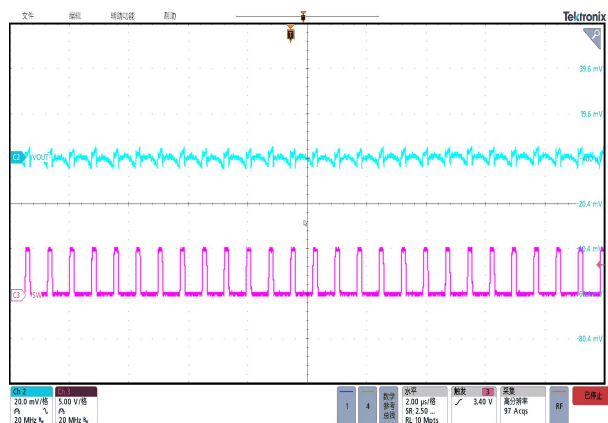
$I_{OUT} = 6.0\text{ A}$, PSM operation

Figure 9. Output voltage ripple



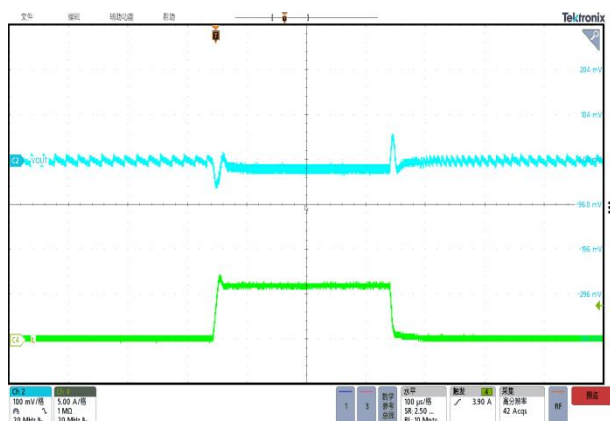
$I_{OUT} = 0\text{ A}$, FPWM operation

Figure 10. Output voltage ripple



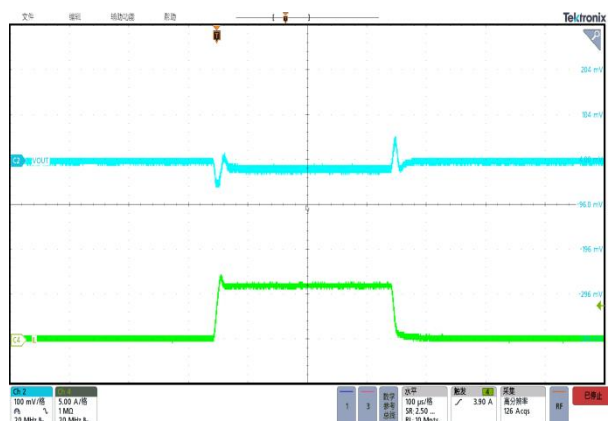
$I_{OUT} = 6.0\text{ A}$, FPWM operation

Figure 11. Load transient



$I_{OUT} = 0.01\text{ A to }6\text{ A}$, PSM

Figure 12. Load transient



$I_{OUT} = 0.01\text{ A to }6\text{ A}$, FPWM

Figure 13. Load transient

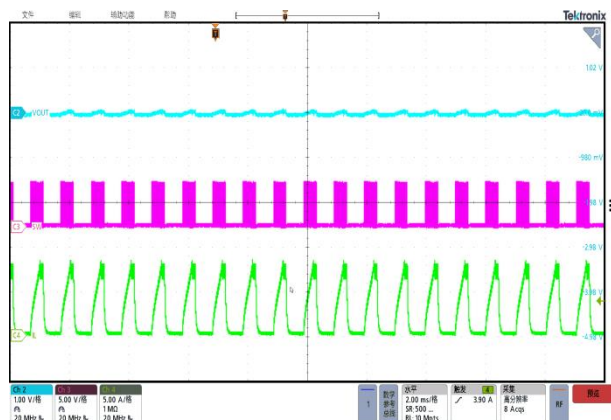


Figure 14. Hiccup short-circuit protection

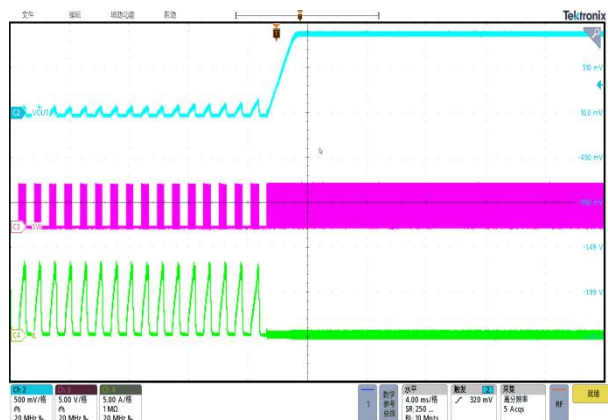
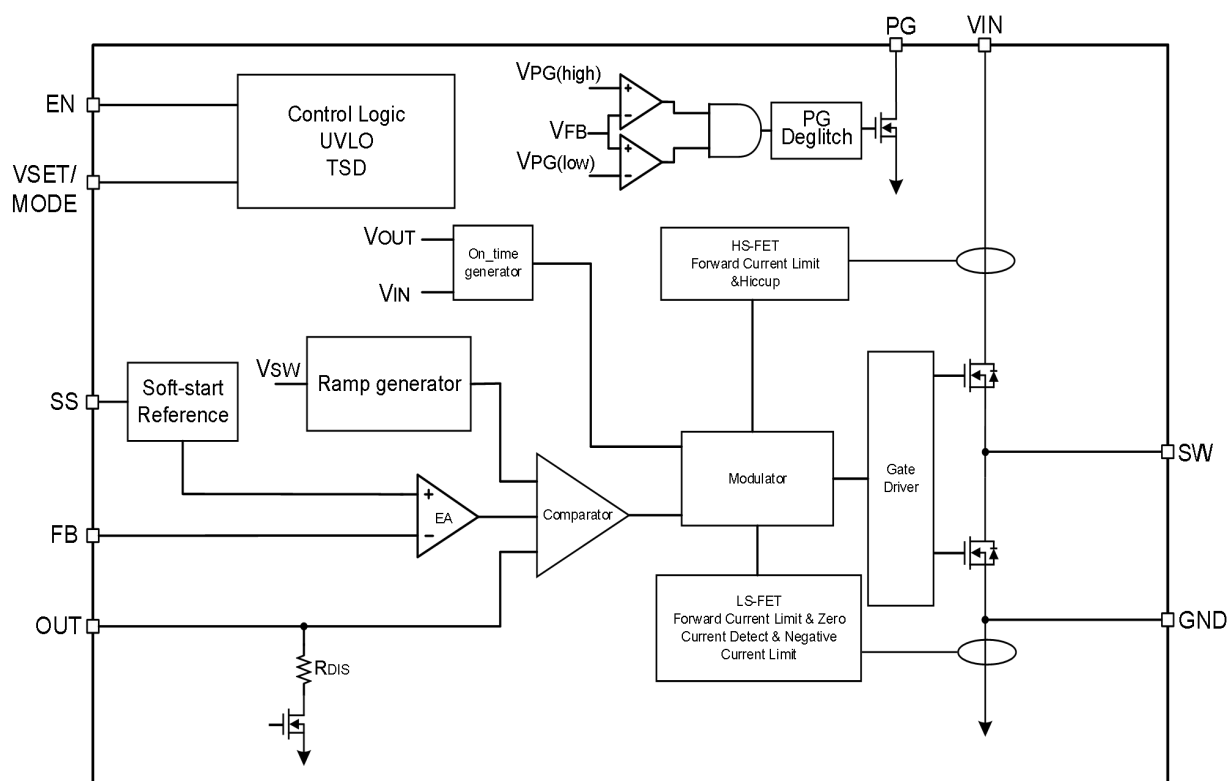


Figure 15. Hiccup short-circuit protection

7. Block Diagram



8. Function Description

8.1. Overview

The DIO6146 is a high-efficiency, high-frequency synchronous buck converter IC with an output current capability of more than 10 A. The device provides a selectable function that allows switching between Forced Pulse-Width Modulation (FPWM) mode and power-save mode through the VSET/MODE pin. When operating in FPWM mode, the DIO6146 achieves ultra-low output ripple. In power-save mode, the device operates in PWM (Pulse-Width Modulation) mode under medium to heavy load conditions with a 1.2 MHz switching frequency to reduce the size of inductor and output capacitor. When the load decreases to a light-load condition, the DIO6146 automatically enters PSM to maintain high efficiency.

The device features fast transient response, a wide input voltage range from 2.4 V to 5.5 V, and very low $R_{DS(on)}$, which effectively reduces conduction losses. The DIO6146 includes a power good indicator signal and adjustable soft-start, and it is capable of 100% duty cycle operation. For fault protection, the DIO6146 integrates hiccup short-circuit protection and thermal shutdown.

8.2. FPWM

After soft-start is completed, the VSET/MODE pin is used as a digital input. When a high level is applied to the VSET/MODE pin, the DIO6146 enters forced PWM (FPWM) mode. Even under light-load conditions, the device switches at 1.2 MHz. This lowers the output voltage ripple and enables straightforward switching frequency filtering for applications that are sensitive to noise. In FPWM mode, efficiency is reduced under light load conditions.

8.3. PSM

The device enters Power-Save Mode (PSM) when the load current drops. When the inductor current reaches 0 A during a switching cycle, which is when it becomes discontinuous, PSM occurs. Equation (1) illustrates the fixed t_{ON} in power-save mode.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 833 \text{ ns} \quad (1)$$

The output voltage increases somewhat over the nominal output voltage when in power-save mode. By raising the output capacitor or inductor value, this impact is reduced.

8.4. 100% duty

When the input voltage approaches the target output voltage, the DIO6146 enters 100% duty-cycle mode, where the high-side MOSFET switch remains continuously on. This feature enables ultra-long runtime in battery-powered applications by fully utilizing the entire battery voltage range. The minimum input voltage required to maintain the minimum output voltage can be calculated using the following equation:

$$V_{IN,MIN} = V_{OUT} + (R_{DS(ON)} + R_L) \times I_{OUT,MAX} \quad (2)$$

where:

- $V_{IN,MIN}$, is the minimum input voltage required to maintain the output voltage.

- $I_{OUT,MAX}$ is the maximum output current.
- $R_{DS(ON)}$ is the on-resistance of the high-side FET.
- R_L is the inductor DC resistance (DCR).

8.5. Soft start

The DIO6146 device features an enable delay (t_{Delay}) before switching begins upon power-up. If the SS pin is unconnected, the internal soft-start circuit controls the output voltage ramp, with soft-start times of 0.5 ms, 1 ms, 1.5 ms, or 2 ms depending on the version.

When a capacitor C_{SS} is connected from the SS pin to GND, the specific ramp time (t_{Ramp}) is set by:

$$t_{Ramp} = 20 \mu A \times C_{SS} / 0.9 V (ms) \quad (3)$$

If the device is set to shutdown, undervoltage lockout, or thermal shutdown, the internal resistor pulls the SS pin to GND. Recovery from these states triggers a new startup sequence.

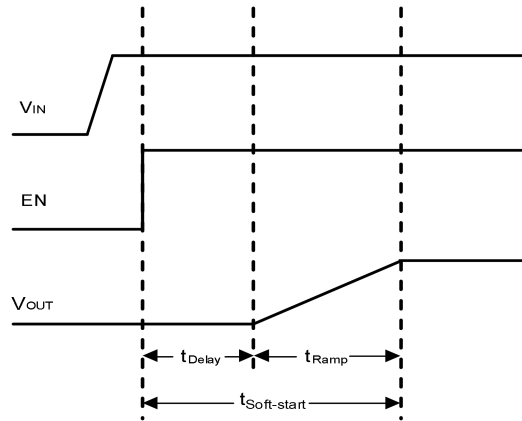


Figure 16. Soft-start sequence

Soft start prevents excessive inrush current and ensures a smooth output voltage ramp. It also prevents excessive voltage drop on primary batteries and rechargeable batteries with high internal impedance.

The DIO6146 can initiate into an output capacitor that has been pre-biased. It ramps the output voltage to its nominal value, starting with the supplied bias voltage.

8.6. Short-circuit protection

8.6.1. Switch current limit and hiccup short-circuit protection

DIO6146A series devices support switch current limit with HICCUP short-circuit protection. By setting a switch current limit, the device may avoid taking too much current from the input voltage rail or battery due to high inductor current. A shorted or saturated inductor, a large load, or a shorted output circuit situation can all result in excessive current. Cycle after cycle, the high-side MOSFET is switched off, and the low-side MOSFET is turned on when the inductor current reaches the threshold I_{LIM} , and the inductor current ramps down to the low-side MOSFET current limit.

The device stops switching after the high-side MOSFET current limit is triggered 32 times. After a typical delay time of 800 μs , the device then restarts automatically using an inbuilt soft-start. HICCUP short-circuit protection

is the term for this. Until the high-load condition disappears, the device keeps operating in this mode.

8.6.2. Latching short-circuit protection

DIO6146B series devices support latching short-circuit protection. If the device encounters a high load or a short-circuit condition, it does not stop switching but continuously operates in current limit mode. Once the device detects that the FB voltage falls below 0.2 V, the device stops switching and enters the latch-off state. Toggling the EN pin (EN off followed by EN on) or removing and reapplying the input voltage unlatches the device and it resumes normal operation.

8.7. Undervoltage lockout (UVLO)

Undervoltage lockout (UVLO) is used when the input voltage is less than V_{UVLO} to prevent the device from malfunctioning at low input voltages. When the device is in UVLO, it ceases switching and the output voltage pull-down is active. The device restarts with an internal soft-start when the input voltage stabilizes. The internal register values are kept during UVLO.

8.8. Thermal shutdown (TSD)

The device enters thermal shutdown, ceases switching, and initiates the output voltage pull down when the junction temperature rises over T_{JSD} . With an inbuilt soft-start, the device returns to normal operation when the temperature drops by thermal shutdown hysteresis(T_{hys}).

8.9. Device functional modes

8.9.1. Enable and disable (EN)

The EN pin needs to be set to logic High to turn on the device. The internal power switches and the whole control circuitry are turned off in shutdown mode (EN = Low). The EN pin must not be left floating in versions without an internal pull-down resistor..

8.9.2. Output pull down

The purpose of the output discharge function is to ensure that the output voltage is reduced according to the defined setting and maintained close to 0 V when the device is disabled. Output discharge is activated when the input voltage falls below the UVLO threshold or during thermal shutdown, or when the EN pin is pulled low.

8.9.3. Power good

The device features an open-drain power-good pin, which is specified to sink up to 1 mA of current. The power-good output requires a pull-up resistor connected to any voltage rail below 5.5 V. PG has a 34 μ s deglitch delay.

By connecting the PG signal to the EN pin of other converters, the PG signal can be used to sequence multiple power rails. If the PG pin is not used, it should be left floating.

Table 1. PG function

Device Conditions		PG Logic Status	
		HIGH	LOW
Enable	$0.9 \times V_{OUT_NOM} \leq V_{OUT} \leq 1.1 \times V_{OUT_NOM}$	√	
	$V_{OUT} < 0.9 \times V_{OUT_NOM}$ or $V_{OUT} > 1.1 \times V_{OUT_NOM}$		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$1.8\text{ V} < V_{IN} < V_{UVLO}$		√
Power supply removal	$V_{IN} < 1.8\text{ V}$	undefined	

8.9.4. Voltage setting and mode selection (VSET/MODE)

The DIO6146 can be configured for adjustable output voltage or fixed output voltage according to individual application requirements, with one device model containing multiple fixed output voltage options and adjustable output voltage options.

During the enable delay (t_{Delay}) period, the device configuration is set by an external resistor connected to the VSET/MODE pin through an internal R2D (resistor-to-digital) converter. Table 2 lists these options. This configures the positive input of the error amplifier (EA) to either the VFB voltage (typical value 0.6 V) or the selected output voltage.

Table 2. Voltage selection

The Resistor On The VSET/MODE Pin (E96 series, ±1% Accuracy, 200 ppm/°C or Lower)	Fixed or Adjustable Output Voltage
249 kΩ or logic high level	Adjustable (through resistor divider on FB pin).
205 kΩ	1.60 V
162 kΩ	1.50 V
133 kΩ	1.35 V
105 kΩ	1.20 V
86.6 kΩ	Reserved
68.1 kΩ	1.00 V
56.2 kΩ	0.90 V
44.2 kΩ	0.85 V
36.5 kΩ	0.80 V
28.7 kΩ	0.70 V
23.7 kΩ	0.60 V
18.7 kΩ	0.50 V
15.4 kΩ	0.45 V
12.1 kΩ	0.40 V
10 kΩ or logic low level	Adjustable (through resistor divider on FB pin).

The R2D converter features an internal current source that applies current to the external resistor, along with an internal ADC that reads back the resulting voltage level. The output voltage is set according to this level. After the R2D conversion is complete, the current source is turned off to prevent current flow through the external resistor. Ensure that additional leakage current paths from this pin to GND during R2D conversion are less than 20 nA and capacitance is less than 30 pF; otherwise, an incorrect value will be set. If the device is configured as a fixed output voltage converter, the FB pin must be directly connected to the output terminal.

After the startup cycle (t_{startup}), different operating modes can be selected. When VSET/MODE is set to a logic high level, the device operates in Forced PWM mode. Otherwise, the VSET/MODE resistor pulls the pin to a low level and the device operates in power-save mode.

9. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

9.1. Typical application

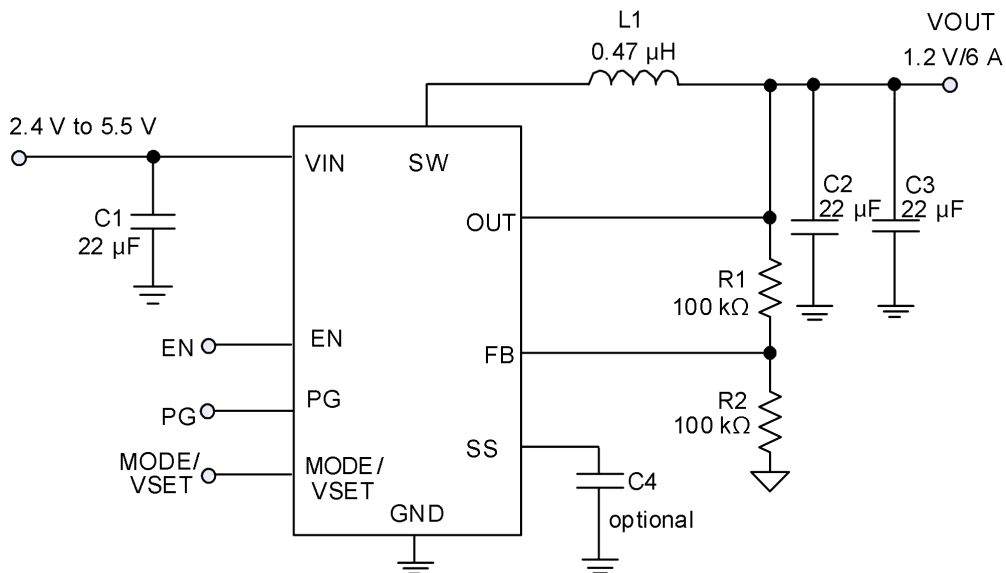


Figure 17. Typical application circuit (DIO6146X06)

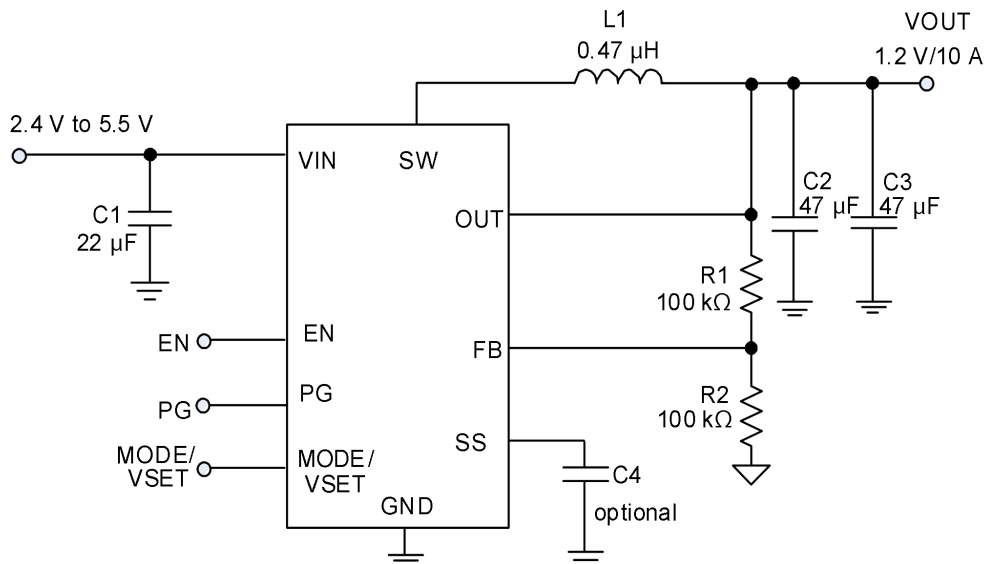


Figure 18. Typical application circuit (DIO6146X10)

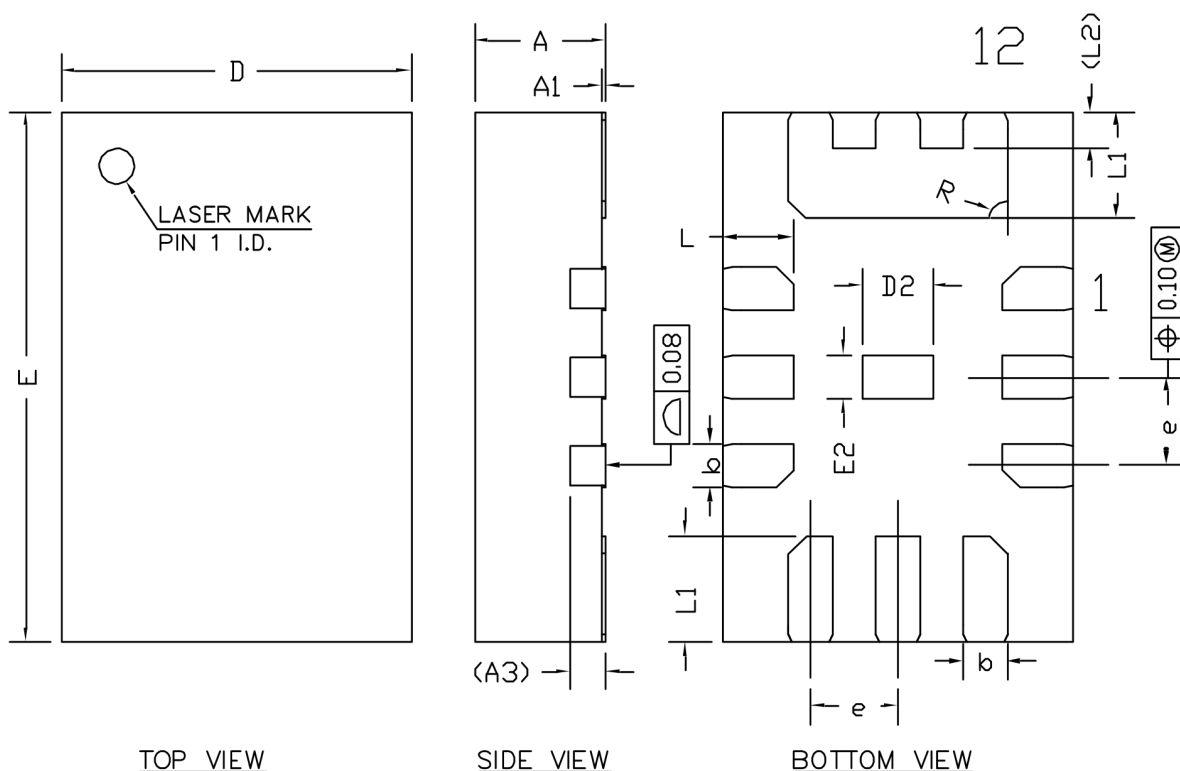
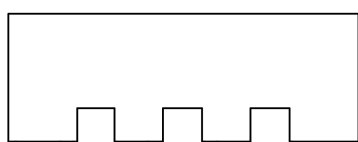
Table 3. Design parameters

Design Parameter	Example Value
Input voltage	2.4 V to 5.5 V
Output voltage	1.2 V
Maximum output current	10 A

Table 4. List of components

Reference	Description	Manufacturer
C1	CAP, CERM, 10 μ F, 10 V, $\pm$ 10%, X7R, 0805, GCM21BR71A106KE22L	MURATA
C2	CAP, CERM, 22 μ F, 10 V, $\pm$ 20%, X7R, 0805, GRM21BZ71A226ME15L	MURATA
L1	470 nH Shielded Molded Inductor 15.7 A 3.7 m Ω , XGL5020-471MEC	Coilcraft
C4	Open	Any
R1	100 k Ω , chip resistor, 1/16 W, 1%, size 0402	Std
R2	100 k Ω , chip resistor, 1/16 W, 1%, size 0402	Std

10. Physical Dimensions: QFN2*3-12



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	2.90	3.00	3.10
D2	0.35	0.40	0.45
E2	0.20	0.25	0.30
e	0.40	0.50	0.60
L	0.35	0.40	0.45
L1	0.55	0.60	0.65
L2	0.200 REF		
R	0.100 REF		

Disclaimer

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