Analog Matrix Switch

FEATURES

- Contains Control Latches, Address Decoding
- Very Short Setup Time and Hold Time
- Wide Voltage Range: 4.5V~13.2V
- 12Vpp Analog Signal
- Ron Maximum 65Ω @VDD=12V，25°C
- Ron≤ 10Ω @VDD=12V，25°C
- Low Distortion, All-CMOS Switch
- Small Feedthrough and Crosstalk
- Independent Analog and Digital Reference Voltage Sources

PRODUCT DESCRIPTION

The MS8816P contains an 8×16 analog switch array, 7-to-128 address decoding and latch circuits. Through different address signals, 128 switches can be addressed. A logic level "1" or "0" input at the DATA port can turn on or turn off the analog switch. The analog signal range is from VDD to VEE. The CS pin also allows expansion of the chip's switch array.

APPLICATIONS

- Keypad Systems
- PBX Systems
- Analog/Digital Multiplexers
- Audio/Video Switches
- Mobile Devices
- Test Equipment

ORDERING GUIDE

Part Number	Package Option	Marking
MS8816P	LQFP44	MS8816P

BLOCK DIAGRAM

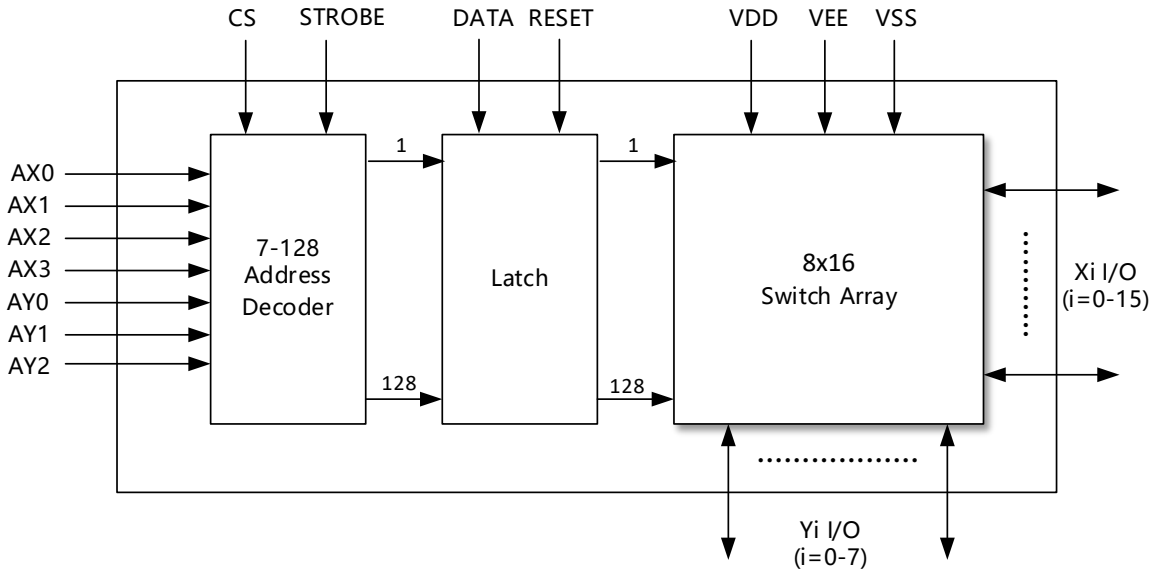
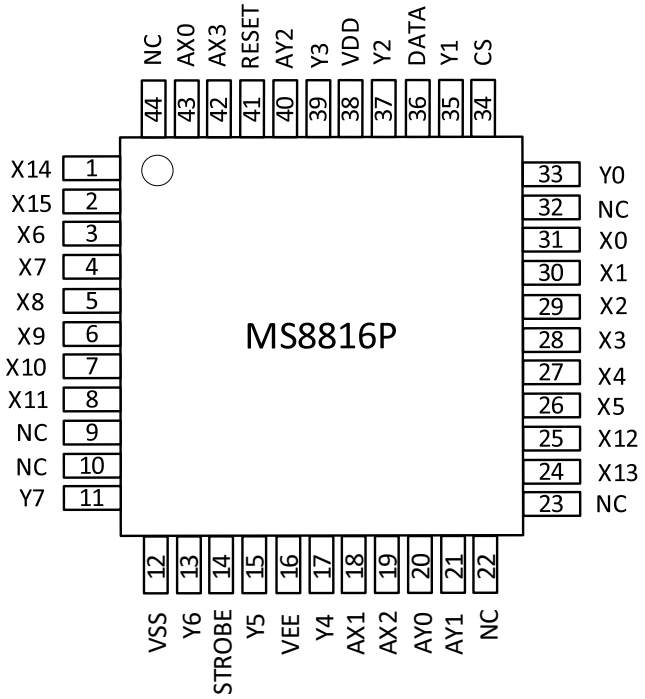


TABLE of CONTENTS

FEATURES 1
PRODUCT DESCRIPTION 1
APPLICATIONS 1
ORDERING GUIDE 1
BLOCK DIAGRAM 1
TABLE of CONTENTS 2
PIN CONFIGURATION 3
ABSOLUTE MAXIMUM RATINGS 5
ESD Caution 5
RECOMMENDED OPERATING CONDITIONS 5
ELECTRICAL CHARACTERISTICS 6
FUNCTION DESCRIPTION 9
PACKAGE OUTLINE DIMENSIONS 11
MARKING and PACKAGING SPECIFICATION 12

PIN CONFIGURATION



Pin	Name	Type	Description
1,2	X14, X15	I/O	Analog Port X14, X15. Connected to Switch Array X14 and X15 Rows
3-8	X6-X11	I/O	Analog Port X6-X11. Connected to Switch Array X6-X11 Rows
9, 10	NC	-	No Connection
11	Y7	I/O	Analog Port Y7. Connected to Switch Array Y7 Row
12	VSS	-	Digital Ground
13	Y6	I/O	Analog Port Y6. Connected to Switch Array Y6 Row
14	STROBE	I	STROBE Port. Enables Address and Data. Before STROBE High Level, Address Must Remain Stable; Before STROBE Falling Edge, Data Must Remain Stable. Active High.
15	Y5	I/O	Analog Port Y5. Connected to Switch Array Y5 Column
16	VEE	-	Negative Power Supply
17	Y4	I/O	Analog Port Y4. Connected to Switch Array Y4 Column
18, 19	AX1, AX2	I	Address Lines AX1 and AX2
20, 21	AY0, AY1	I	Address Lines AY0 and AY1
22, 23	NC	-	No Connection
24, 25	X13, X12	I/O	Analog Port X13 and X12. Connected to Switch Array X13 and X12 Rows

Pin	Name	Type	Description
26-31	X5-X0	I/O	Analog Port X5-X0. Connected to Switch Array X5-X0 Rows
32	NC	-	No Connection
33	Y0	I/O	Analog Port Y0. Connected to Switch Array Y0 Column
34	CS	I	Chip Select. Active High
35	Y1	I/O	Analog Port Y1. Connected to Y1 Switch Array
36	DATA	I	Data Input. High Level Turns On Switch; Low Level Turns Off Switch. Active High
37	Y2	I/O	Analog Port Y2. Connected to Switch Array Y2 Column
38	VDD	-	Positive Power Supply
39	Y3	I/O	Analog Port Y3. Connected to Switch Array Y3
40	AY2	I	Address Line AY2
41	RESET	I	Turns Off All Switches. High Level Reset
42, 43	AX3, AX0	I	Address Lines X3, X0
44	NC	-	No Connection

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn' t represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	VDD	-0.3 ~ 16	V
	VSS	-0.3 ~ VDD+0.3	V
Analog Input Voltage	VINA	-0.3 ~ VDD+0.3	V
Digital Input Voltage	VIN	VSS-0.3 ~ VDD+0.3	V
Port Current	I	±15	mA
Storage Temperature	Tstg	-65 ~ +150	°C
Power Dissipation	PD	0.6	W

ESD Caution



Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Parameter Range	Unit
Operating Temperature	TA	-40 ~ 85	°C
Power Supply Voltage	VDD	4.5 ~ 13.2	V
	VSS	VEE ~ VDD-4.5	V
Analog Input Voltage	VINA	VEE ~ VDD	V
Digital Input Voltage	VIN	VSS ~ VDD	V

ELECTRICAL CHARACTERISTICS

DC Parameters

VEE=VSS=0V, VDD = 12V, TA=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current	IDD	All Digital Inputs VIN = VSS or VDD		1	100	μ A
		All Digital Inputs VIN = 2.4V+VSS，VSS=7.0V		0.4	1.5	mA
		All Digital Inputs VIN = 3.4V		5	15	mA
Leakage Current	IOFF	/Vxi-Vyj/=VDD - VEE		±1	±500	nA
Input Low Level	VIL	VSS=6.5V，VEE = 0V			0.8+VSS	V
Input High Level	VIH	VSS=6.5V，VEE = 0V	2+VSS			V

DC Parameters-On Resistance

Parameter	Symbol	Condition		25°C		70°C		85°C		Unit
				Typ	Max	Typ	Max	Typ	Max	
On Resistance	RON	VSS=VEE=0V，VDC=VDC/2，/Vxi-Vyj/=0.4V	VDD=12V	45	65		75		80	Ω
			VDD=10V	55	75		85		90	
			VDD=5V	120	185		215		225	
On Resistance Difference Between Two Switches	⊿RON	VDD=12V，VDC=VDD/2，VSS=VEE=0V，/Vxi-Vyj/=0.4V		5	10		10		10	Ω

AC Parameters-Crosspoint Performance

VEE=-7V, VDD=5V, VSS=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switch Capacitance	CS	f=1MHz		20		pF
Coupling Capacitance	CF	f=1MHz		0.2		pF
Frequency Response Bandwidth, Channel “ON” 20log(Vout/Vxi)=-3dB	F3dB	Switch “ON”，VINA = 2Vpp Sine Wave, RL = 1kΩ		45		MHz

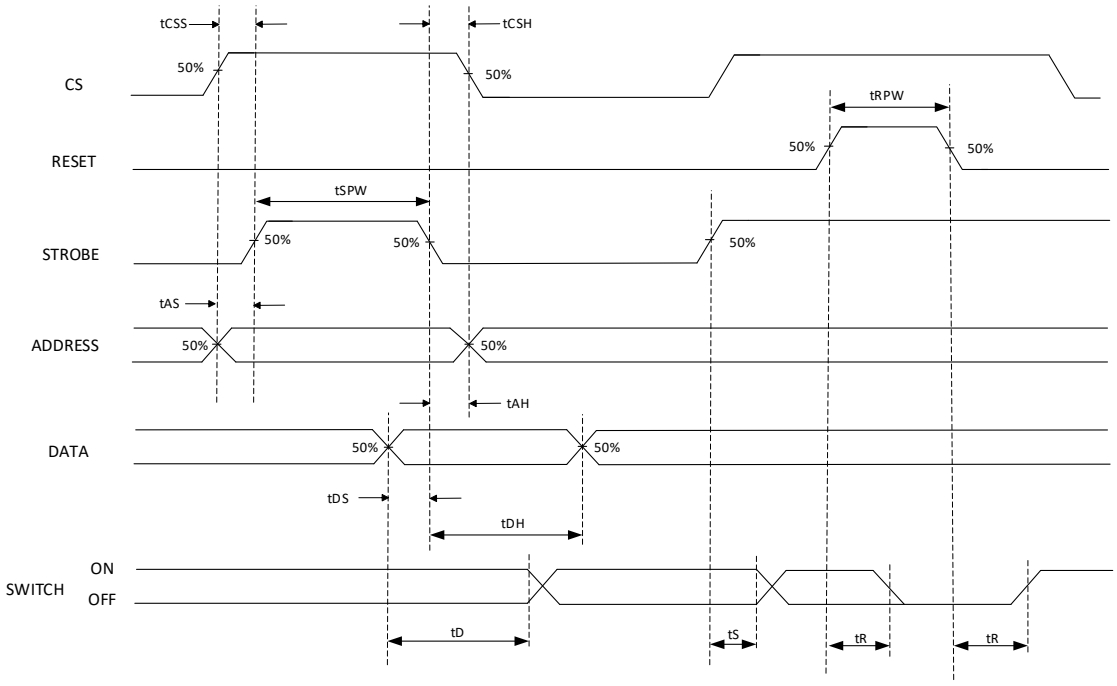
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Total Harmonic Distortion	THD	Switch "ON", VINA=2Vpp, f=1kHz Sine Wave, RL=1kΩ		0.01		%
Isolation, Channel "OFF"	FDT	All Switches "OFF", VINA=2Vpp, f=1kHz Sine Wave, RL=1kΩ		-95		dB
Crosstalk Between Two Channels	Xtalk	VINA=2Vpp, f=10MHz Sine Wave, RL=75Ω		-45		dB
		VINA = 2Vpp, f=10kHz Sine Wave, RL=600Ω		-90		dB
		VINA = 2Vpp, f=10kHz Sine Wave, RL=1kΩ		-85		dB
		VINA = 2Vpp, f=1kHz Sine Wave, RL=10kΩ		-80		dB
Channel Delay	tps	RL=1kΩ, CL=50pF			30	ns

AC Parameters-Timing Control

VEE=-7V, VDD=5V, VSS=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Control Input to Switch Crosstalk (CS, DATA, ADDRES, STROBE)	CXtalk	VIN=3V Square Wave, RIN=1kΩ, RL=10kΩ		30		mVpp
Digital Input Capacitance	CDI	f=1MHz		10		pF
Switching Frequency	FO				20	MHz
DATA to STROBE Setup Time	tDS	RL = 1kΩ, CL=50pF	10			ns
DATA to STROBE Hold Time	tDH	RL = 1kΩ, CL=50pF	10			ns
ADDRES to STROBE Setup Time	tAS	RL = 1kΩ, CL=50pF	10			ns
ADDRES to STROBE Hold Time	tAH	RL = 1kΩ, CL=50pF	10			ns
CS to STROBE Setup Time	tCSS	RL = 1kΩ, CL=50pF	10			ns
CS to STROBE Hold Time	tCSH	RL = 1kΩ, CL=50pF	10			ns
STROBE Pulse Width	tSPW	RL = 1kΩ, CL=50pF	20			ns
RESET Pulse Width	tRPW	RL = 1kΩ, CL=50pF	40			ns
STROBE to Switch State Delay	tS	RL = 1kΩ, CL=50pF		40	100	ns
DATA to Switch State Delay	tD	RL = 1kΩ, CL=50pF		50	100	ns
RESET to Switch State Delay	tR	RL = 1kΩ, CL=50pF		35	100	ns

Timing Diagram



FUNCTION DESCRIPTION

The MS8816P is an 8×16 analog switch matrix circuit. The switch matrix has 8 columns in the Y direction and 16 rows in the X direction. When a switch is off, absolute isolation is achieved between the corresponding X row and Y row of the analog switch array; when a switch is on, the X row and Y row are connected.

The control register consists of a 128-bit writable RAM, and the bit position can be selected through the address input lines (AX0-AX3, AY0-AY2). Data is written into the memory through the DATA port. When STROBE and CS inputs are high, different data can be written to the DATA port, and data is latched on the falling edge of STROBE. To ensure valid writing, the data port must remain stable before the falling edge. When a logic "1" is written to a memory cell, the corresponding crosspoint switch is turned on; when a logic "0" is written to a memory cell, the corresponding crosspoint switch is turned off. When data is written to the memory, the state of the crosspoint at the addressed memory location changes. The remaining switches keep their previous states. By writing different data in the controller, different combinations of X and Y can be obtained. When the RESET input is logic "1", regardless of the CS state, all switches are turned off and the memory data is cleared. The two voltage reference pins (VSS and VEE) can provide negative analog signals for the MS8816P. The digital signal voltage range is from VDD to VSS, and the analog signal voltage range is from VDD to VEE. If only one power supply is available, VSS and VEE can be connected together.

Address Decoding

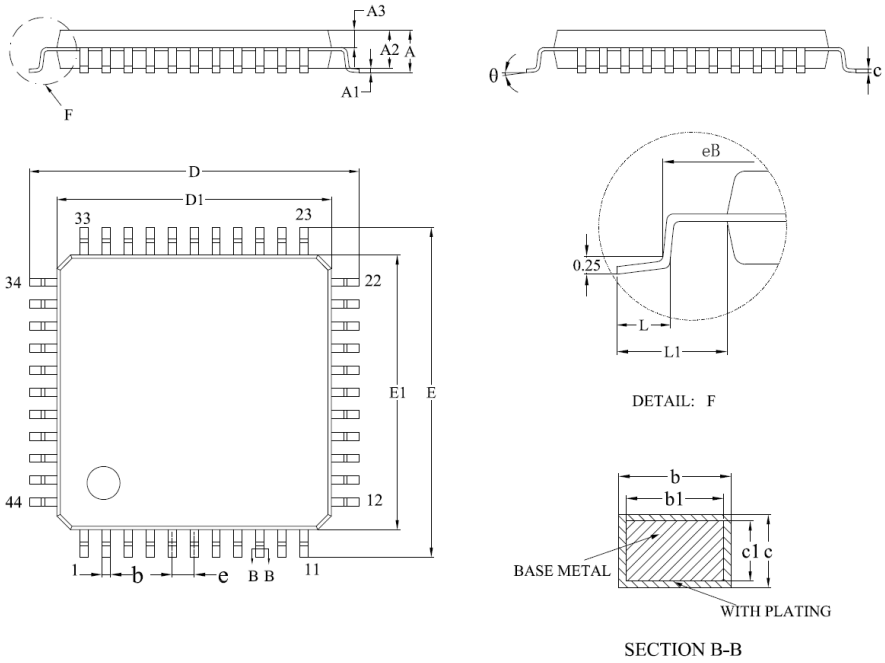
Under the control of the STROBE and CS enable signals, 7 address lines are input to the 7-to-128 address decoder. DATA is buffered and then used as the input to all memories. When RESET is low and CS is high, data and addresses can be written to the latch, and data is latched on the falling edge of STROBE. Data can be written only when STROBE is high, and switches can be turned on and off. To ensure valid data writing, data should remain stable before the falling edge of STROBE.

Address Decoding Truth Table

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
1	1	1	0	0	0	0	X13-Y0
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	X14-Y0
1	1	1	1	0	0	0	X15-Y0
0	0	0	0	0	0	0	X0-Y1
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y1
0	0	0	0	0	0	0	X0-Y2
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y2
0	0	0	0	0	0	0	X0-Y3
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y3
0	0	0	0	0	0	0	X0-Y4
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y4
0	0	0	0	0	0	0	X0-Y5
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y5
0	0	0	0	0	0	0	X0-Y6
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y6
0	0	0	0	0	0	0	X0-Y7
↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	X15-Y7

PACKAGE OUTLINE DIMENSIONS

LQFP44



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.05	-	11.25
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name : MS8816P

Product Code : XXXXXX

2. Marking Drawing Demand

Laser marking, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Plate	Plate/Box	Piece /Box	Box/Carton	Piece/Carton
MS8816P	LQFP44	160	10	1600	6	9600

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