2 Port eUSB2.0 to USB2.0 Redriver

Features

- Compliance with USB2.0 and eUSB2 (rev 1.2)
- Support for low-speed (LS), full-speed (FS), high-speed (HS) modes
- Register access protocol receptor capable
- Dual independent redrivers
- Support for host and device modes (DRD)
- I^2C device interface for more configurations
- Device variants
  - eUSB2 1.0 V or 1.2 V signaling interface
  - Four eUSB2 trace loss compensation levels for different product form-factors: 2.5, 5, 7.5, and 10 inches
- Optional BC1.2 CDP battery charging and detection support

Applications

- Smartphone
- Tablet
- Notebook
- Wearables
- eUSB2 to USB2.0 redriver function in platforms

Package Information

Part Number	Package	Body Size
DIO36620	QFN-20	3 mm × 3 mm

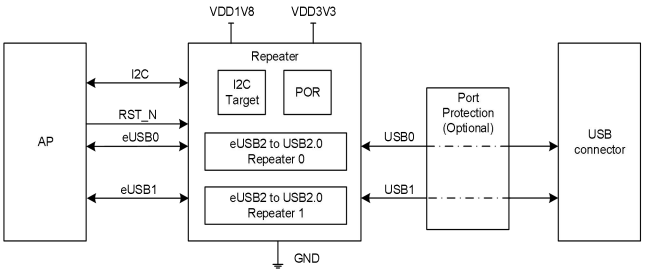
Description

The DIO36620 is a USB compliant dual-channel eUSB2 to USB2.0 redriver supporting both device and host modes.

The DIO36620 implements redriver mode (eUSB2 to USB2.0 redriver) and supports link power management functionality. The DIO36620 is designed to comply with USB2.0 and eUSB2 standards. It supports all three speeds/data rates: low speed (1.5 Mbps), full speed (12 Mbps), and high speed (480 Mbps).

The DIO36620 is available in green package QFN-20. The device is specified over ambient temperature range from -40°C to 85°C. It is suitable for all eUSB2 to USB2.0 platforms.

Simplified Schematic



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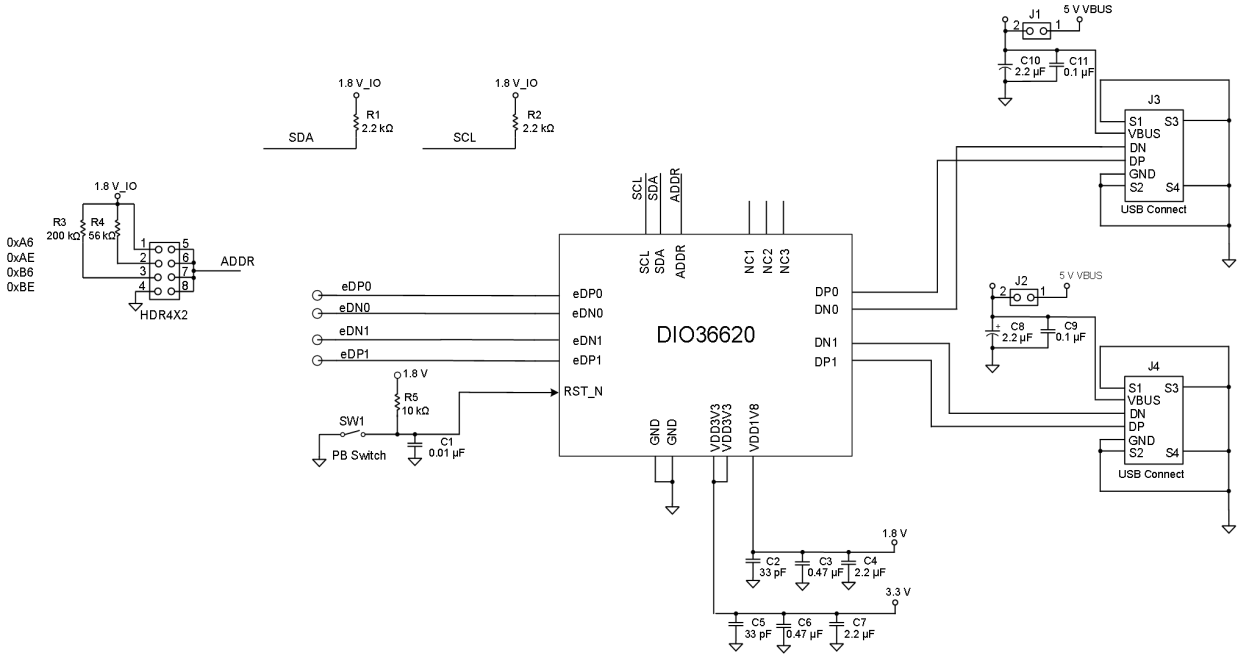
Typical Application Circuit



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Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO36620LN20	D3FB	3	Green	-40°C to 85°C	QFN3×3-20	Tape and Reel, 5000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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1. Pin Assignment and Functions

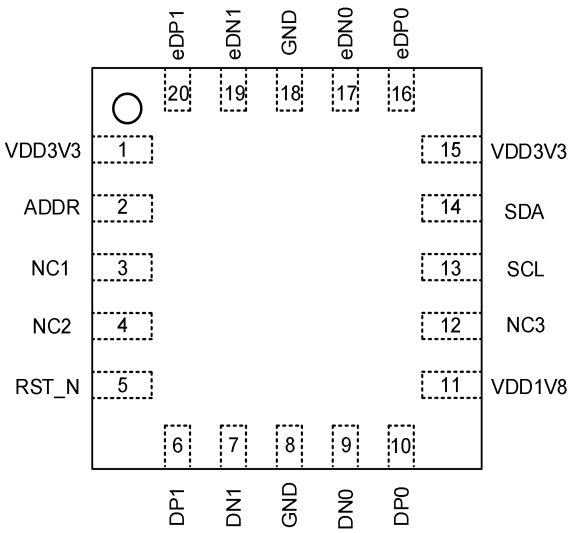

Figure 1. QFN3×3-20 (Top view)

Pin No.	Pin Name	Type	Associated ESD Supply	Description
1, 15	VDD3V3	PWR		The 3.3 V power supply has decoupling capacitors of 2.2 µF, 0.47 µF and 33 pF installed close to this pin on the PCB.
2	ADDR	Digital I/O	VDD1V8	One pin for I^2C target address selection (sampled once after POR or RST).
3, 4, 12	NCX(1)	NC		Not connected.
5	RST_N	Digital I/O	VDD1V8	It is an active-low input signal meant to perform IC reset operation.
6	DP1	Analog I/O	VDD3V3	Positive terminal of USB2.0 analog transceiver interface D1+ pin has an internal 500 kΩ pull-down resistor enabled under all situations.
7	DN1	Analog I/O	VDD3V3	Negative terminal of USB2.0 analog transceiver interface D1- pin has an internal 500 kΩ pull-down resistor enabled under all situations.
8, 18	GND	GND		Ground.
9	DN0	Analog I/O	VDD3V3	Negative terminal of USB2.0 analog transceiver interface D0- pin has an internal 500 kΩ pull-down resistor enabled under all situations.
10	DP0	Analog I/O	VDD3V3	Positive terminal of USB2.0 analog transceiver interface D0+ pin has an internal 500 kΩ pull-down resistor enabled under all situations.

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11	VDD1V8	PWR		The 1.8 V power supply has decoupling capacitors of 2.2 μF, 0.47 μF and 33 pF installed close to this pin on the PCB.
13	SCL	Digital Input	VDD1V8	I^2C clock input. There is no internal pull-up resistor, and an external pull-up resistor to I^2C pull-up voltage must be used on the PCB.
14	SDA	Digital I/O	VDD1V8	I^2C data input/output. There is no internal pull-up resistor, and an external pull-up resistor to I^2C pull-up voltage must be used on the PCB.
16	eDP0	Analog I/O	VDD1V8	Positive terminal of eUSB2 analog transceiver interface.
17	eDN0	Analog I/O	VDD1V8	Negative terminal of eUSB2 analog transceiver interface.
19	eDN1	Analog I/O	VDD1V8	Negative terminal of eUSB2 analog transceiver interface.
20	eDP1	Analog I/O	VDD1V8	Positive terminal of eUSB2 analog transceiver interface.

Note:

(1) X = 1, 2, 3.

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2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Ratings	Unit
VDD3V3	3V3 supply voltage		-0.5 to 4	V
VDD1V8	1V8 supply voltage		-0.5 to 2.4	V
V_{IN}	Input voltage	SCL, SDA	-0.5 to 2.4	V
		RST_N	-0.5 to 2.4	
		eDP, eDN	-0.5 to 2.4	
		DP, DN	-0.5 to 5.5	
		ADDR	-0.5 to 2.4	
T_{STG}	Storage temperature		-60 to 150	°C

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Unit
VDD3V3	3V3 supply voltage		2.85	3.3	3.63	V
VDD1V8	1V8 supply voltage		1.62	1.8	1.98	V
t_{VDD_rampup}(1)	Supply voltage ramp-up time, between 0 V and VDD3V3 min/VDD1V8 min		0.3		10	ms
VDD1V8	I^2C interface pull-up voltage(2)	1.8 V voltage reference used for I^2C pins (same as VDD1V8 supply)	VDD1V8 min	VDD1V8	VDD1V8 max	V
V_{IN}	Input voltage	SCL, SDA	-0.3		1.98	V
		RST_N	-0.3		1.98	V
		eDP, eDN	-0.3		1.32	V
		DP, DN	-0.3		3.63	V
		ADDR	-0.3		1.98	V
T_A(1)	Ambient temperature	Operating in standing air environment – mobile/computing IOT market	-40		85	°C

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Symbol	Parameter		Min	Typ	Max	Unit
T_J(3)	Junction temperature	Captured mainly to ensure that simulation is carried out in this temp corner	-40		125	°C

Note:

(1) Guaranteed by design.

(2) V_{PULLUP} is used to refer to I^2C pull-up voltage in the following sections. VDD1V8 refers to internal voltage reference used by DIO36620 for determining the logic levels of SCL/SDA pins.

(3) DIO36620 is simulated for functionality up to junction temperature of 125°C, but it is not guaranteed to meet the power/current consumption specifications.

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
HBM	ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	ANSI/ESDA/JEDEC JS-002	±500	V

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5. Electrical Characteristics

5.1. Device characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{Startup}$(1)	Device start-up time	Time for device operation including I²C accesses once both supply voltages are within recommended operating levels			1	ms
t_{sw_reset}(1)	Time for software reset to complete	Supply voltages are valid			0.5	ms
t_{CFG}(1)	Device parameter (re)configuration time	Time for parameter (re)configuration values to take effect after I²C programming (or RAP initialization)			0.5	ms
t_{dpss_Exit}(1)	Time duration that host has to wait before issuing further commands when DIO36620 is exiting DPSS				275	µs
$I_{supply,3V3}$	VDD3V3 supply current	Deep standby			7	µA
		Connect detect mode			20	µA
		L2 mode			36	µA
		L1 mode			36	µA
		Active LS/FS mode			25	mA
		Active HS mode (eUSB to USB direction); no de-emphasis; only Rx EQ enabled on eUSB2/USB2.0 pins; 90 Ω termination on USB2.0 pins and 80 Ω on eUSB2 pins			16	mA
		Active HS mode (eUSB to USB direction) de-emphasis 3dB on USB2.0; Rx EQ enabled on eUSB2/USB2.0 pins; 85 Ω termination on USB2.0 side and 80 Ω termination on eUSB2 side			22	mA
		Active HS mode (USB to eUSB direction); no de-emphasis; only Rx EQ enabled on eUSB2/USB2.0 pins; 90 Ω termination on USB2.0 pins and 80 Ω on eUSB2 pins			6	mA
		Active HS mode (USB to eUSB direction); de-emphasis 3dB on USB2.0; Rx EQ enabled on eUSB2/USB2.0 pins; 85 Ω termination on USB2.0 side and 80 Ω termination on eUSB2			8	mA

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		side				
$I_{supply,1V8}$	VDD1V8 supply current	Deep standby for mobile/computing/IOT market			100	μA
		Connect detect mode			260	μA
		L2 mode			260	μA
		L1 mode			1.6	mA
		Active LS/FS mode			18	mA
		Active HS mode (eUSB to USB direction); no de-emphasis; only Rx EQ enabled on eUSB2/USB2.0 pins; 90 Ω termination on USB2.0 side and 80 Ω on eUSB2 side, 400 mV USB2.0 output swing			120	mA
		Active HS mode (eUSB to USB direction); de-emphasis 3dB on USB2.0; Rx EQ enabled on eUSB2/USB2.0 pins; 85 Ω termination on USB2.0 pins and 80 Ω termination on eUSB2 pins			130	mA
		Active HS mode (USB to eUSB direction); no de-emphasis; only Rx EQ enabled on eUSB2/USB2.0 pins; 90 Ω termination on USB2.0 side and 80 Ω on eUSB2 side, 400 mV USB2.0 output swing			70	mA
		Active HS mode (USB to eUSB direction); de-emphasis 3dB on USB2.0; Rx EQ enabled on eUSB2/USB2.0 pins; 85 Ω termination on USB2.0 pins and 80 Ω termination on eUSB2 pins			80	mA
$I_{backpower,\ 3V3}$	Back power current when VDD3V3 is at ground	Current going into SCL pin when SCL is tied to VDD1V8 max			1	μA
		Current going into SDA pin when SDA is tied to VDD1V8 max			1	μA
		Current into RST_N pin when RST_N is tied to VDD1V8 max			1	μA
$I_{backpower,\ 1V8}$	Back power current when VDD1V8 is at ground	Current going into SCL pin when SCL is tied to VDD1V8 max			1	μA
		Current going into SDA pin when SDA is tied to VDD1V8 max			1	μA

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		Current into RST_N pin when RST_N is tied to VDD1V8 max			1	μA
I_{INRUSH_3V3}(1)	Inrush current during VDD3V3 ramp up from 0 V to final value				1	mA
I_{INRUSH_1V8}(1)	Inrush current during VDD1V8 ramp up from 0 V to final value				1	mA

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

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5.2. USB2.0 and eUSB2 characteristics

Applicable across operating temperature and power supply ranges as mentioned under recommended operating conditions unless otherwise noted. Typical values are specified at 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IH_LF_USB2.0}$	USB2.0 low/full speed high-level input voltage		2			V
$V_{IL_LF_USB2.0}$	USB2.0 low/full speed low-level input voltage				0.8	V
$V_{OL_LF_USB2.0}$	USB2.0 low/full speed low-level output voltage				0.3	V
$V_{OH_LF_USB2.0}$	USB2.0 low/full speed high-level output voltage		2.8		3.7	V
$Z_{SO_LF_USB2.0}$	USB2.0 transmit output series resistance		40.5		49.5	Ω
$V_{OP_TX_USB2.0}$	USB2.0 HS Tx output signal swing	Measured on DP/DN pin with no de-emphasis with 90 Ω (nominal) differential termination; I²C setting = 0	315	350	385	mV
		I²C setting = 1	360	400	440	mV
		I²C setting = 2	405	450	495	mV
		I²C setting = 3	450	500	550	mV
		I²C setting = 4	495	550	610	mV
		I²C setting = 5	540	600	660	mV
		I²C setting = 6	585	650	715	mV
		I²C setting = 7	630	700	770	mV
$R_{RCV_DIF_USB2.0}$	USB2.0 HS Rx differential receiver termination	Measured on DP/DN pin; I²C setting = 4	72	80	88	Ω
		I²C setting = 3	75	85	95	Ω
		I²C setting = 2	77	90	100	Ω
		I²C setting = 1	80	95	105	Ω
		I²C setting = 0	85	100	110	Ω
$V_{SQ_RX_USB2.0}$	USB2.0 HS Rx squelch detection threshold	Measured on DP/DN pin; with 90 Ω nominal differential termination; I²C setting = 0	25	50	75	mV
		I²C setting = 1	40	65	90	mV
		I²C setting = 2	60	85	110	mV
		I²C setting = 3	70	95	120	mV
		I²C setting = 4	85	110	135	mV
		I²C setting = 5	100	125	150	mV

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		I²C setting = 6	115	140	165	mV
		I²C setting = 7	130	155	180	mV
$V_{DIS_HS_USB2.0}$	USB2.0 HS Rx disconnect detection threshold	Measured on DP/DN pin under disconnect condition; I²C setting = 0	525	575	625	mV
		I²C setting = 1	625	675	725	mV
		I²C setting = 2	725	775	825	mV
		I²C setting = 3	825	875	925	mV
$t_{RISE_TX_FS_USB2.0}$(1)	USB2.0 FS Tx Rise/Fall time control	Measured on DP/DN pin (10% ~ 90% of final voltage level); with 90 Ω nominal differential termination; I²C setting = 0	8		20	ns
		I²C setting = 1	4		14	ns
$R_{RCV_DIF_eUSB2}$	eUSB2 HS Rx differential receiver termination	Measured on eDP/eDN pin	72	80	88	Ω
$V_{OP_TX_eUSB2}$	eUSB2 HS Tx output signal swing	Measured on eDP/eDN pin with no de-emphasis with 80 Ω (nominal) differential termination; I²C setting = 0	140	180	220	mV
		I²C setting = 1	160	200	240	mV
		I²C setting = 2	180	220	260	mV
		I²C setting = 3	200	240	280	mV
$V_{SQ_RX_eUSB2}$	eUSB2 HS Rx squelch threshold as measured on eDP/eDN pin	Measured on eDP/eDN pin; with 80 Ω nominal differential termination; I²C setting = 0	25	50	75	mV
		I²C setting = 1	40	65	90	mV
		I²C setting = 2	60	85	110	mV
		I²C setting = 3	70	95	120	mV
$V_{OL_LF_eUSB2}$	eUSB2 LS/FS low-level output voltage	(0.15 x internally derived 1.2 V reference from VDD1V8)			0.18	V
$V_{OH_LF_eUSB2}$	eUSB2 LS/FS high-level output voltage	(0.85 x internally derived 1.2 V reference from VDD1V8)	1.02			V
$V_{IL_LF_eUSB2}$	eUSB2 LS/FS low-level input voltage	(0.35 x internally derived 1.2 V reference from VDD1V8)			0.42	V
$V_{IH_LF_eUSB2}$	eUSB2 LS/FS high-level input voltage	(0.65 x internally derived 1.2 V reference from VDD1V8)	0.78			V
$Z_{TXSRC_LF_eUSB2}$	eUSB2 LS/FS Transmit output impedance		28		60	Ω
$V_{OVP, Th}$	VBUS Overvoltage detector on DP and DN pins	Low-to-high transition	4.2	4.6	5.2	V
		High-to-low transition	3.9	4.4	5.0	V

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V_{CRS}	USB2.0 LS cross-over voltage		1.3		2.0	V

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

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5.3. I²C characteristics

Applicable across operating temperature and power supply ranges as recommended operating conditions unless otherwise noted. Typical values are specified at 25°C, unless otherwise noted. I²C can operate in 1.8 V.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{I2C}	I²C clock frequency		100	400	1000	kHz
R_{PULLUP}	I²C interface pull-up resistors on SCL/SDA lines	System requirement	0.567	2.2	2.83	kΩ
V_{IH}	High-level input voltage	Standard mode, 1.8 V	0.7 × VDD1V8			V
V_{IL}	Low-level input voltage	Standard mode, 1.8 V	-0.3		0.3 × VDD1V8	V

Note:

(1) Specifications subject to change without notice.

5.4. ADDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH1}	High-level input voltage	Pin connected to VDD1V8	0.9 × VDD1V8		VDD1V8 + 0.3	V
V_{IH2}	High-level input voltage	Rext = 56 kΩ (10% resistor) pull-up to VDD1V8	0.575 × VDD1V8		0.725 × VDD1V8	V
V_{IH}	High-level input voltage	Rext = 200 kΩ (10% resistor) pull-up to VDD1V8	0.275 × VDD1V8		0.425 × VDD1V8	V
V_{IL}	Low-level input voltage	Pin connected to GND			0.1 × VDD1V8	V
I_{bckcur}	Back current on pin when there is no power	VDD1V8 = 0 (no power supply to RST_N input pad)			1	μA
I_{IL}	Pin leakage current	Pin connected directly to GND			5	μA

Note:

(1) Specifications subject to change without notice.

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5.5. RST_N characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.8 V IO operation	1.2			V
V_{IL}	Low-level input voltage	1.8 V IO operation			0.3	V
I_{bckcur}	Back current on pin when there is no power	VDD1V8 = 0 (no power supply to RST_N input pad)			1	μA
I_{IL}	Pin leakage current	Pin connected directly to GND			5	μA

Note:

(1) Specifications subject to change without notice.

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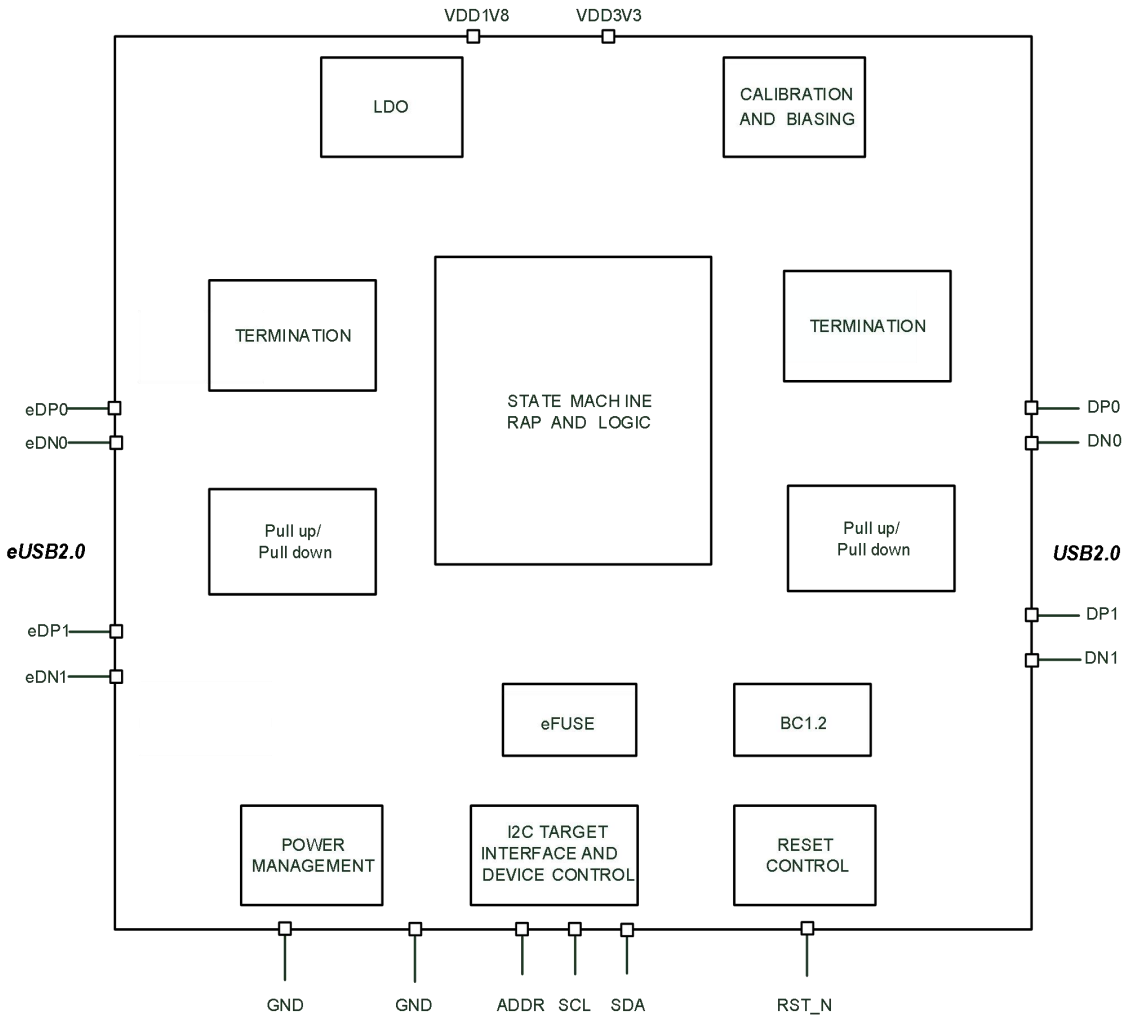
6. Block Diagram



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7. Functional Description

7.1. Mode of operations

Which mode the DIO36620 runs in is governed by the redriver setup, the path state and whether a connection is present. Table 1 summarizes which internal blocks stay powered for each mode.

Table 1. Status of design blocks in different power modes

Power Mode	I²C Interface	FS/LS Data Paths	HS Data Paths
OFF	OFF	OFF	OFF
Deep standby	ON	OFF	OFF
Connect detect (Detached condition)	ON	ON (SE detector only)	OFF
L1 mode	ON	ON (SE detector only)	HS OFF; only SE detector is ON
L2 mode	ON	ON (SE detector only)	HS OFF; only SE detector is ON
Active LS/FS	ON	ON	OFF
Active HS	ON	OFF	ON

7.2. Reset Behavior

Two kinds of reset are available in the DIO36620: power-on reset (POR) and software-initiated reset.

When the DIO36620 device is held in reset, the SCL and SDA I/O pins are placed in a high-impedance state, ensuring that the I²C bus remains unaffected and preventing any potential alteration or corruption of data on the bus.

7.3. I²C Interface

The DIO36620 behaves purely as an I²C target. It answers I²C commands in every mode, provided VDD3V3 and VDD1V8 are powered. 10-bit addressing, the I²C software reset command, and the general call address (including its acknowledgement) are all unsupported. ACK is returned for every one of the 128 register offsets, even though some offsets are reserved or undefined in the register map.

Any I²C sequence that reads or writes a run of consecutive registers is called a transaction. Consecutive simply means incrementing address, whether or not each address is defined. A communication may chain several transactions—to different targets or repeatedly to the same target with different offsets—separated by repeated-START conditions; any transaction form permitted by the I²C specification is accepted.

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7.3.1. I²C target address

The DIO36620's 7-bit I²C target address is specified in below table. Bits 3 and 4 are configurable and can assume one of four possible values depending on the state of the quaternary address selection pin (ADDR).

Table 2. DIO36620 target address definition

ADDR Pin Configuration	Bit 7	Bit 6	Bit 5	ADDR		Bit 2	Bit 1	Bit 0
				Bit 4	Bit 3			
Connected to 1.8 V supply directly	1	0	1	0	0	1	1	R/W
Connected to 1.8 V supply via a 56 kΩ (±10%) pull-up resistor	1	0	1	0	1	1	1	R/W
Connected to 1.8 V supply via a 200 kΩ (±10%) pull-up resistor	1	0	1	1	0	1	1	R/W
Connected to GND directly	1	0	1	1	1	1	1	R/W

7.4. eUSB2 redriver

This subsystem comprises the eUSB2 analog front-end circuitry, the redriver state machine, the USB2.0 analog front-end circuitry, and the associated power management circuits. The USB2.0 DP/DN pins have internal 500 kΩ pull-down resistors that remain enabled under all conditions.

The DIO36620 is designed to operate either as a host redriver or as a peripheral redriver. Figure 2 illustrates the role transition and the corresponding arcs that enable role change.

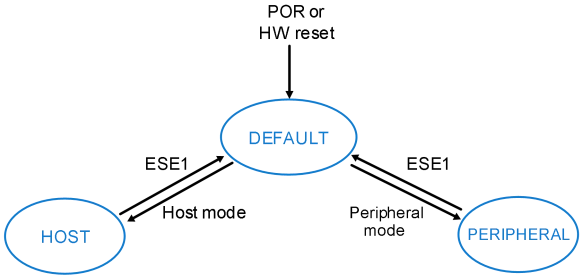

Figure 2. Role state transitions

Figure 3 illustrates the usage of the eUSB2 Host redriver in a typical host platform application.

On the device side, the redriver interfaces with a USB2.0 peripheral redriver, either connected directly or through a cable/channel topology. On the system side, it interfaces with the host controller via the eUSB2 PHY.

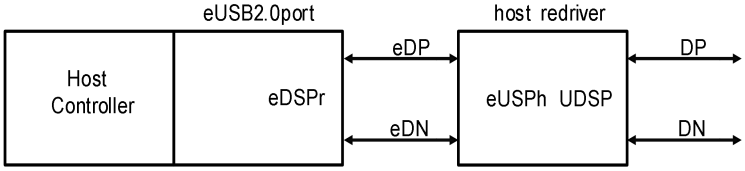

Figure 3. DIO36620 as eUSB2 host redriver

Figure 4 illustrates the usage of the eUSB2 peripheral redriver in a typical peripheral application environment.

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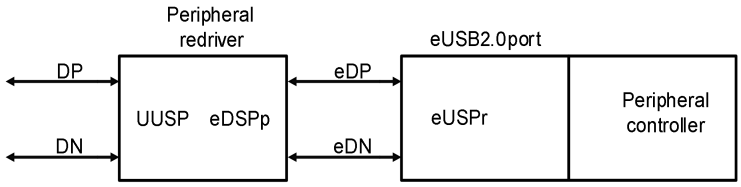

Figure 4. DIO36620 as eUSB2 peripheral redriver

The DIO36620 implements advanced power management techniques to minimize overall power consumption across the various operating modes. It supports USB link power management, including the L1 and L2 power states.

RAP access is restricted to registers intended for customer use. The I^2C register selects the allowed access type. No internal arbitration exists between a RAP access and an I^2C access targeting the same register. Therefore, the system implementation must avoid issuing simultaneous accesses to prevent register overwrites, which could result in incorrect device behavior or responses.

The DIO36620 accepts RAP messages at any time. Although the host is expected to issue RAP messages primarily during initialization, the device does not restrict the use of RAP commands for reading status registers or updating control registers, provided that the DIO36620 is in a mode where customer I^2C registers are accessible.

7.5. Overvoltage protection on USB2.0 DP/DN pins

A dedicated overvoltage protection (OVP) circuit monitors the overvoltage on the USB2.0 DP/DN pins and reacts on its own, with no host involvement. A typical overvoltage sequence runs as follows:

1. The DIO36620 monitors the DP/DN pins for voltages exceeding the $V_{OVP,Th}$ threshold (Low-to-high transition) and disables the USB2.0 analog I/O as long as the overvoltage condition persists.

2. After the voltage drops back below $V_{OVP,Th}$, the DIO36620 re-enables the USB2.0 analog I/O path.

3. Since the channel is opened, the link between the SoC host and the attached USB2.0 peripheral redriver is lost.

4. To restore the link, the host can choose:

    a. Issue a CM.Reset to trigger a USB Bus Reset, or

    b. Issue a Port reset to the local redriver and toggle VBUS to re-establish the connection and resume data transport.

Where:

(1) Option a is the quickest and least intrusive recovery, though success depends on the fault type.

(2) Option b is guaranteed to restore the link, but takes longer.

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7.6. BC1.2 support

The DIO36620 provides built-in support for the CDP feature, letting a connected mobile device recognize the downstream port and draw an elevated charging current. Implementation-wise, a controlled voltage source can be connected to the USB2.0 DN pin by an I^2C register bit. The host normally enables it via I^2C while no USB connection exists; once a connection is detected, the device turns the source off and clears the control bit by itself.

This feature is intended for use in host redriver mode only; however, the DIO36620 does not block activation of this feature while operating as a device redriver.

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8. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

8.1. Use cases

The DIO36620 is intended for a wide range of USB interface scenarios. On one side, it attaches to a host or device controller equipped with an eUSB2 PHY; on the other side it connects to a connector/cable assembly or to a companion interface IC. The connector may be a custom type, USB Standard-A, Standard-B, Micro-B or USB Type-C.

In every scenario, host-side I²C initialization after POR or reset is not mandatory: the device is fully operational with its POR/default register values and needs no I²C configuration at all to function.

The following figures illustrate representative topologies. They are simplified and do not show every channel component (supply decoupling, ESD protection, common-mode filters, etc.).

8.1.1. Direct connector

The simplest arrangement: the redriver drives the connector directly. It fits general-purpose IoT products and some computing designs. The I²C interface may be left unconnected, leaving the part to run on POR/default settings from power-up.

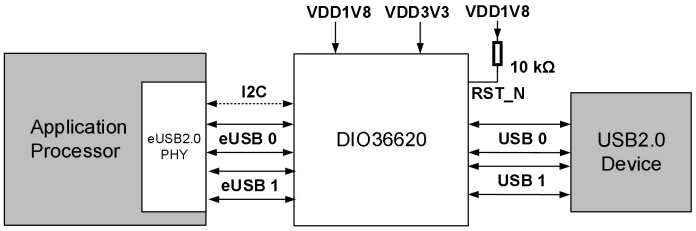

Figure 5. Use case 1 - direct interfacing

8.1.2. Interface via USB protection IC

The USB data lines may encounter hazardous voltages, e.g. behind a USB-C receptacle. In some cases, I²C can be left unconnected, while the DIO36620 is expected to start operating automatically after POR with its default register settings. The protection IC must be chosen carefully, its switch path introduces $R_{DS(on)}$ and capacitance, so its USB2.0 signal attenuation must be acceptable, and the default power-up behavior of the combined chain needs analysis.

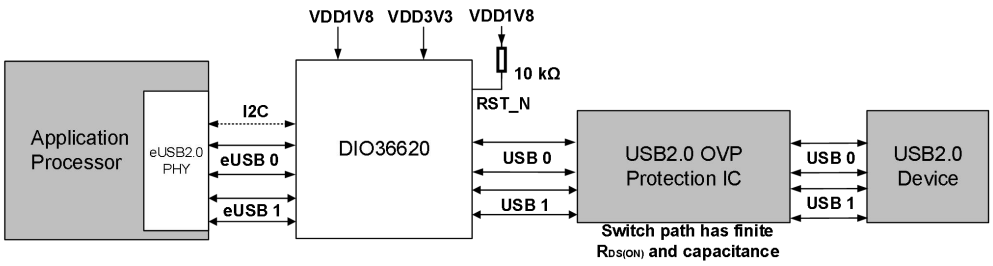

Figure 6. Use case 2 - interfacing via protection IC

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8.1.3. Interface to connector via passive signal switch

This connectivity scheme allows multiple debug and communication signals to be routed to the same connector. The I^2C interface can be left unconnected, with POR/default settings taking effect after power-up. The passive switch must have low insertion loss, and its power-up behavior must be verified. The RST_N pin requires an external 10 kΩ pull-up resistor, either on the SoC or on the PCB.

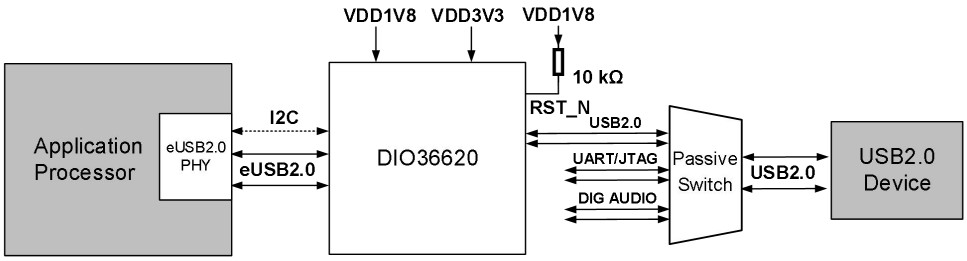

Figure 7. Use case 3 - interfacing via passive switch

8.2. Power supply requirements

The DIO36620 requires two power supplies, VDD3V3 and VDD1V8, to operate. The device remains non-functional until both supplies have ramped up and reached their valid operating ranges. No specific power-on or power-off sequencing is required. Additionally, the two supplies may have different ramp-up and ramp-down rates, with the supply ramp limits specified in *Recommended Operating Conditions*.

The DIO36620 does not exhibit back-powering issues (For example VDD nodes being powered through non-power pins).

Power supply decoupling capacitors should be placed and soldered as close as possible to the corresponding power pins.

8.3. Grounding requirements

The DIO36620 features two ground pins: GND.

These pins should be connected to the PCB ground plane to ensure low ground noise in the application.

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9. Register

The device is controlled and monitored by registers accessible via the I²C bus. All registers can be accessed in standard mode or fast mode using single reads or writes. Register bit field types are defined as below table.

Table 3. Register type definitions

Access Type	Description
RW	Bit field can be read and written
WO	Bit field values is written only
RO	Bit field values is read only
RAZ	Bit field contents are read as zero
W1C	Bit field write 1 to clear

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9.1. Register map

Table 4. Register map

Address	Register Name	Type	Reset		Default (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			POR	Software Reset									
0x00	RESERVED	RAZ			00								
0x01	PORT0_RESET CONTROL	RW	•		00								PORT0_SOFT_RESET
0x02	PORT0_LINK_CTRL1	RW	•	•	00	PORT0_SPEED_CTRL		PORT0_ROLE_CTRL			PORT0_OPERATIONAL_MODE		
0x03	PORT0_LINK_CTRL2	RW	•	•	00							Auto Resume Enable	PORT0_FORCE_ESE1
0x04	PORT0_EUSB2_RX_CTRL	RW	•	•	20			PORT0 eUSB2 HS Rx Squelch Detection Threshold			PORT0 eUSB2 HS Rx Equalization		
0x05	PORT0_EUSB2_TX_CTRL	RW	•	•	10			PORT0 eUSB2 HS Tx Output Swing				PORT0 eUSB2 HS Tx De-Emphasis	
0x06	PORT0_USB2_RX_CTRL	RW	•	•	40		PORT0 USB2 Rx Squelch Detection Threshold				PORT0 USB2 HS Rx Equalization		
0x07	PORT0_USB2_TX_CTRL1	RW	•	•	22			PORT0 USB2 HS Tx De-emphasis Bit Duration			PORT0 USB2 HS Tx De-emphasis		
0x08	PORT0_USB2_TX_CTRL2	RW	•	•	63		PORT0 USB2 FS	PORT0 USB2 HS Rise/Fall Time			PORT0 USB2 HS Tx Output Swing		

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Address	Register Name	Type	Reset		Default (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			POR	Software Reset									
							rise/fall time						
0x09	PORT0_USB2_HS_TERM	RW	•	•	02						PORT0 USB2 HS Termination Control		
0x0A	PORT0_USB2_DISCONNT_TH	RW	•	•	00							PORT0 USB2 HS Disconnect Detection Threshold	
0x0B	RESERVED	RW			XX								
0x0C	RESERVED	RW			XX								
0x0D	PORT0_RAP_SIGN	RW	•	•	00	PORT0_RAP_Signature							
0x0E	PORT0_VDX_CTRL	RW	•	•	00								PORT0_VDx_ Enable
0x0F	PORT0_DEVICE_STATUS	RO	•	•						PORT0 Speed of Operation Status	PORT0 Redriver Status		
0x10	PORT0_LINK_STATUS	RO	•	•							PORT0 Device and Link Status		
0x11	RESERVED	RAZ			XX								
0x12	RESERVED	RAZ			XX								
0x13	REVISION_ID	RO			00	BASE = b'0000				METAL_= b'0000			
0x14	CHIP_ID_0	RO			62								
0x15	CHIP_ID_1	RO			36								
0x16	CHIP_ID_2	RO			10								

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Address	Register Name	Type	Reset		Default (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			POR	Software Reset									
0x20	RESERVED	RAZ			XX								
0x21	PORT1_RESET_CTRL	RW	•		00								PORT1_SOFT_RESET
0x22	PORT1_LINK_CTRL1	RW	•	•	00	PORT1_SPEED_CTRL		PORT1_ROLE_CTRL			PORT1_OPERATIONAL _MODE		
0x23	PORT1_LINK_CTRL2	RW	•	•	00							AUTO RESUME ENABLE	PROT1_FORCE_SEE1
0x24	PORT1_EUSB2_RX_CTRL	RW	•	•	20			PORT1 eUSB2 HS RX Squelch Detection Threshold			PORT1 eUSB2 HS Rx Equalization		
0x25	PORT1_EUSB2_TX_CTRL	RW	•	•	10			PORT1 eUSB2 HS Tx Output Swing				PORT1 eUSB2 HS Tx De-emphasis	
0x26	PORT1_USB2_RX_CTRL	RW	•	•	40		PORT1 USB2 RX Squelch Detection Threshold				PORT1 USB2 HS Rx equalization		
0x27	PORT1_USB2_TX_CTRL1	RW	•	•	22			PORT1 USB2 HS Tx De-emphasis Bit Duration			PORT1 USB2 HS Tx De-emphasis		
0x28	PORT1_USB2_TX_CTRL2	RW	•	•	63		PORT1 USB2 HS rise/fall time	PORT1 USB2 HS rise/fall time			PORT1 USB2 HS Tx Output Swing		
0x29	PORT1_USB2_HS_TERM	RW	•	•	02						PORT1 USB2 HS Termination Control		

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Address	Register Name	Type	Reset		Default (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			POR	Software Reset									
0x2A	PORT1_USB2_DISCONNT_TH	RW	•	•	00							PORT1 USB2 HS Disconnect Detection Threshold	
0x2B	PORT1_DEVICE_STATUS	RO	•	•						PORT1 Speed of Operation States		PORT1 Redriver Status	
0x2C	PORT1_LINK_STATUS	RO	•	•							PORT1 Device and Link Status		
0x2D	PORT1_RAP_SIGN	RW	•	•	00	PORT1_RAP_Signature							
0x2E	PORT1_VDX_CTRL	RW	•	•	00								PORT1_VDX_CTRL

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9.2. I²C register and description

9.2.1. Functional register

The offset addresses with defined bit fields correspond to functional registers and can be accessed by the I²C controller at any time after a POR. For normal operation, these registers provide sufficient control to configure the IC to known working conditions. Customers are advised not to write reserved values into the register bit fields. Reads from reserved bit fields may not return the same value that was written. Functional behavior is not guaranteed if reserved fields are written or otherwise misused.

9.2.1.1. RESERVED

Address: 0x00

Bit	Bit Name	Type	Default	Description
7:0	RSVD	RAZ	b'00000000	Reserved.

9.2.1.2. PORT0_RESET CONTROL

Address: 0x01

Bit	Bit Name	Type	Default	Description
7:1	RSVD	RAZ	b'0000000	Reserved.
0	PORT0_SOFT_RESET	R/W	b'0	This bit is self-clearing. Writing a '1' to this bit initiates a software reset, and the bit automatically clears to '0'. All read/write registers are reset to their POR default settings. Writing a '0' to this bit has no effect. Reads of this bit always return '0'.

This register is meant to initiate reset of the chip via I²C write.

9.2.1.3. PORT0_LINK_CTRL1

Address: 0x02

Bit	Bit Name	Type	Default	Description
7:6	PORT0_SPEED_CTRL	RW	b'00	This bit field defines the POR default setting for the USB2.0 speed. 00: Manage the speed via Auto negotiation. 01: LS/FS only. 10: Reserved. 11: Reserved.
5:4	PORT0_ROLE_CTRL	RW	b'00	Determines the redriver role. 00: Dual role. Supports negotiation of eUSB2 port configuration for both host and device roles. This is the standard operating mode managed through eUSB2 exchanges initiated by the host. 01: Force Host role. When the bits are set to '01', the redriver is forced into the USB Host role, overriding any configuration commands received via eUSB2. However, the redriver still acknowledges configuration messages from the host.

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				10: Force Device role. When these bits are set to '10', the redriver is forced into the USB Device/Peripheral redriver role, overriding any configuration commands received via eUSB2. However, the redriver still acknowledges configuration messages from the host. 11: Reserved. The forced host/device role setting is applicable only when Link Control 1[2:0] bits are set to '2'.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT0_OPERATIONAL_MODE	RW	b'000	The bits define the operational mode of the redriver. 0: Auto negotiation on the link (mode determined via control messages and link negotiation). 1: Deep standby mode (eUSB2 pins are pulled down, USB2.0 pins are held in weak pull-down condition and I^2C register contents are preserved). 2: Connect detect state. Used to force the redriver into its Connect. Detect state (refer to eUSB2 specification). The action takes effect only at the moment the register is written. If an overriding condition, such as RST_N = 0, exists, the write operation is discarded, even after the condition is cleared. In this scenario, the role control field (register 0x02) must have only one bit set. These bits specify the role the redriver should assume. This command directs the redriver to enter the corresponding the Connect.Detect state based on the role control setting. Once the state transition is complete, the redriver automatically responds to the eUSB2/USB2.0 bus conditions accordingly. 3: Compliance Mode (HS L0 condition). This action is equivalent to receiving the Control Message CM.Test, enabling the system to force the redriver into the HS.L0 state. The roles are determined by the role control bits. In this case, only a single bit must be set in the role control field; if both or neither bit is set, the command is ignored. 4 to 7: Reserved.

This register is used to force the redriver role and fix the operating speed.

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9.2.1.4. PORT0_LINK_CTRL2

Address: 0x03

Bit	Bit Name	Type	Default	Description
7:2	RSVD	RAZ	b'000000	Reserved.
1	Auto Resume Enable	RW	b'0	0: Follow eUSB specification. 1: Enable Auto resume and asynchronous wake-up feature.
0	PORT0_ FORCE_ESE1	RW	b'0	Bit to force Extended SE1 signaling. 0: No action. 1: Self-clearing bit. When written to 1, Redriver generates extended SE1 onto the eUSB2 pins. Typically, only the host redriver initiates this action upon detecting a HS disconnect. However, this feature enables the system to enforce an extended SE1 signaling state through the I^2C interface as required.

This register configures a specific feature of the redriver.

9.2.1.5. PORT0_EUSB2_RX_CTRL

Address: 0x04

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT0 eUSB2 HS Rx Squelch Detection Threshold	RW	b'10	The bits set the squelch detector threshold level for transitioning from Low to High on eUSB2 HS signaling pins. 00: 50 mV. 01: 65 mV. 10: 85 mV. 11: 95 mV. All settings are within ±25 mV of the specified nominal values. The squelch detector incorporates a 10 mV hysteresis to enhance noise immunity.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT0 eUSB2 HS Rx Equalization	RW	b'000	The bits set the nominal eUSB2 receive equalization gain at 240 MHz relative to the DC gain. All settings are accurate within ±1 dB of the specified nominal values. 000: 0 dB. 001: 1 dB. 010: 2 dB 011: 3 dB. 100: 4 dB. 101 to 111: Reserved.

This register configures the eUSB2 receiver equalization and squelch detection threshold settings.

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9.2.1.6. PORT0_EUSB2_TX_CTRL

Address: 0x05

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT0 eUSB2 HS Tx Output Swing	RW	b'01	The bits configure the output signal swing for high-speed (HS) signaling on the eUSB2 transmitter side when the interface is properly terminated. 00: 180 mV. 01: 200 mV. 10: 220 mV. 11: 240 mV. All settings are within ±40 mV of nominal value mentioned above.
3:2	RSVD	RAZ	b'00	Reserved.
1:0	PORT0 eUSB2 HS Tx de-emphasis	RW	b'00	The bits determine the Tx de-emphasis (nominal) level for HS signaling on eUSB2 pins. The de-emphasis duration is between 0.75 to 1 HS bit time. 00: 0 dB. 01: 1 dB. 10: 2 dB. 11: 3 dB. All settings other than '00' are within ±1 dB of nominal value mentioned above.

The register programs the eUSB2 transmitter output swing and de-emphasis level. (applicable for high-speed signaling only).

9.2.1.7. PORT0_USB2_RX_CTRL

Address: 0x06

Bit	Bit Name	Type	Default	Description
7	RSVD	RAZ	b'0	Reserved.
6:4	PORT0 USB2.0 HS Rx Squelch Detection Threshold	RW	b'100	The 3 bits set the squelch detector threshold level for the Low-to-High transition in HS signaling on USB2.0 pins. 000: Reserved; not for use. 001: 65 mV. 010: 85 mV. 011: 95 mV. 100: 110 mV. 101: 125 mV. 110: 140 mV. 111: 155 mV.

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				All settings are within ±25 mV of nominal value mentioned above Squelch detector implements hysteresis of 10 mV to improve noise immunity.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT0 USB2.0 HS Rx Equalization	RW	b'000	The 3 bits configure the nominal USB2.0 receive equalization gain at 240 MHz relative to the DC gain. All settings are accurate within ±1 dB of the specified nominal values. 000: 0 dB. 001: 1 dB. 010: 2 dB. 011: 3 dB. 100: 4 dB. 101 to 111: Reserved.

This register configures the Rx equalization and squelch detection threshold levels on USB2.0 pins, applicable only to HS signaling.

9.2.1.8. PORT0_USB2_TX_CTRL1

Address: 0x07

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT0 USB2.0 HS Tx De-emphasis Bit Duration	RW	b'10	The bits configure the de-emphasis bit time (UI) for HS signaling on the USB2.0 Tx side. 00: 0. 01: 0.5 UI. 10: 0.8 UI. 11: Reserved. All settings are within ±0.2 UI of nominal value mentioned above.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT0 USB2.0 HS Tx De-emphasis	RW	b'010	The bits determine the Tx de-emphasis (nominal) level for HS signaling on USB2.0 pins. 000: 0 dB. 001: 1 dB. 010: 2 dB. 011: 3 dB. 100: 4 dB. 101: 5 dB. 110: 6 dB. All settings other than '000' are within ±1 dB of nominal value mentioned above.

This register configures the transmit-side parameters, including de-emphasis levels for the USB2.0 side.

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The DIO36620 implements a de-emphasis feature to compensate for channel loss in the high-frequency components of both eUSB2 and USB2.0 signals.

Figure 8 depicts the distinction between the pre-emphasis and de-emphasis functions.

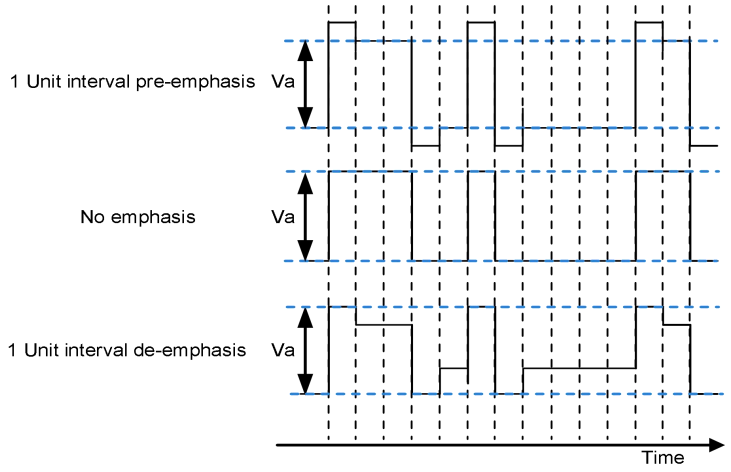

Figure 8. Difference between pre-emphasis and de-emphasis functions

With de-emphasis, when a steady pattern of 0 s or 1 s is transmitted, the output signal swing is reduced according to the configured de-emphasis level. For alternating patterns of 0 s and 1 s, the full signal swing is transmitted, as determined by the nominal transmit signal swing level.

With pre-emphasis, the full signal amplitude is maintained for steady patterns of 0 s or 1 s, while alternating patterns of 0 s and 1 s experience a boosted transmit signal swing according to the pre-emphasis level.

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9.2.1.9. PORT0_USB2_TX_CTRL2

Address: 0x08

Bit	Bit Name	Type	Default	Description
7	RSVD	RAZ	b'0	Reserved.
6	PORT0 USB2.0 FS Rise/Fall Time	RW	b'1	This bit controls the rise and fall times of the FS Tx driver on the USB2.0 pins. 0: 8 to 20 ns. 1: 4 to 14 ns. Load conditions are as defined in USB standard.
5:4	PORT0 USB2.0 HS Rise/Fall Time	RW	b'10	The 2 bits define the Tx driver slew rate for HS signaling on the USB2.0 pins. 00: 500 to 900 ps. 01: 400 to 830 ps. 10: 300 to 760 ps. 11: Reserved. Load conditions are as defined in USB standard.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT0 Tx Output Signal Swing	RW	b'011	The 3 bits specify the Tx output signal swing level for HS signaling on USB2.0 pins (when the interface is terminated). 000: 350 mV. 001: 400 mV. 010: 450 mV. 011: 500 mV. 100: 550 mV. 101: 600 mV. 110: 650 mV. 111: 700 mV. All settings are within ±10% of nominal value mentioned above.

This register configures the transmit-side settings, including the Tx output driver slew rate and output signal swing on the USB2.0 side.

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9.2.1.10. PORT0_USB2_HS_TERM

Address: 0x09

Bit	Bit Name	Type	Default	Description
7:3	RSVD	RAZ	b'00000	Reserved.
2:0	PORT0 USB2.0 HS Termination Control	RW	b'010	The bits set the HS termination on USB2.0 pins, defining the differential impedance. 000: 100 Ω differential. 001: 95 Ω differential. 010: 90 Ω differential. 011: 85 Ω differential 100: 80 Ω differential. 101 to 111: Reserved. All settings are within ±10% of nominal value mentioned above.

This register configures the HS termination values on the USB2.0 pins.

9.2.1.11. PORT0_USB2_DISCONNT_TH

Address: 0x0A

Bit	Bit Name	Type	Default	Description
7:2	RSVD	RAZ	b'000000	Reserved.
1:0	PORT0 HS Disconnect Threshold Level	RW	b'00	The bits determine the HS Disconnect detector threshold level on USB2.0 pins. 00: 575 mV. 01: 675 mV. 10: 775 mV. 11: 875 mV. All settings are within ±50 mV of nominal value mentioned above. The detector implements hysteresis of 30 mV to improve noise immunity.

This register configures the HS disconnect threshold level on the USB2.0 pins.

9.2.1.12. PORT0_RAP_SIGN

Address: 0x0D

Bit	Bit Name	Type	Default	Description
7:0	PORT0 RAP_Signature	RW	b'00000000	0x00: No RAP Access to DIO36620 I²C Registers. 0x37: RAP allowed read only access to Status, REVISION_ID, and Chip ID registers. 0x92: RAP allowed read only access to I²C customer registers. 0x21: RAP allowed write/read access to I²C customer registers. All others: No RAP Access to registers.

The RAP signature controls and restricts RAP command access to the redriver's registers.

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9.2.1.13. PORT0_VDX_CTRL

Address: 0x0E

Bit	Bit Name	Type	Default	Description
7:1	RSVD	RAZ	b'0000000	Reserved.
0	PORT0_VDX_Control	RW	b'0	VDX Control - Host Side Redriver Function. 0: Disable VDX_SRC. 1: Enable VDX_SRC. The host must enable VDX_SRC within 200 ms after a disconnect, and the DIO36620 VDX_SRC circuitry is automatically disabled upon detection of the next connection.

The DIO36620 can indicate that the host system is a USB BC 1.2 CDP to a USB peripheral redriver. This is achieved by activating a current source on the USB DN pin, as defined by the VDM_SRC parameter in the USB BC 1.2 specification.

9.2.1.14. PORT0_DEVICE_STATUS

Address: 0x0F

Bit	Bit Name	Type	Default	Description
7:4	RSVD	RAZ		Reserved.
3:2	PORT0 Speed of Operation	RO		The bits show the current state of redriver speed of operation. 00: LS. 01: FS. 10: HS.
1:0	PORT0 Redriver Status	RO		The bits show the current role played by the redriver. 00: No role determined yet. 01: Device side redriver. 10: Host side redriver.

This register reflects the current state of the redriver functionality. It is a read-only register; any write operation has no effect.

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9.2.1.15. PORT0_LINK_STATUS

Address: 0x10

Bit	Bit Name	Type	Default	Description
7:3	RSVD	RAZ		Reserved.
2:0	PORT0 Device and Link Status	RO		The status bits reflect the device and link state. 000: Deep standby. 001: Connect detect. 010: L1. 011: L2. 100: Active LS/FS (L0) 101: Active HS (L0). 110: Active HS (L0) forced due to USB2.0 compliance mode. 111: This setting represents transitioning condition between different states (For example: Suspend to Resume to L0).

This status register reflects the current state of the redriver device and link. It is read-only, and write operations have no effect.

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9.2.1.16. REVISION_ID

Address: 0x13

Bit	Bit Name	Type	Default	Description
7:4	BASE_STEP	RO	b'0000	Base layer version. 0: 1st version.
3:0	METAL_STEP	RO	b'0000	Metal layer version. 0: 1st version.

The REVISION_ID register contains the silicon revision number. It is a read-only register, and its value remains constant.

9.2.1.17. CHIP_ID_0

Address: 0x14

Bit	Bit Name	Type	Default	Description
7:0	CHIP_ID_0	RO	b'01100010	Lower 8-bit CHIP ID (0x62).

The ID register contains the lower 8 bits of the 16-bit chip part number (3662). It is a read-only register with a fixed value that never changes.

9.2.1.18. CHIP_ID_1

Address: 0x15

Bit	Bit Name	Type	Default	Description
7:0	CHIP_ID_1	RO	b'00110110	Higher 8-bit CHIP ID (0x36).

The ID register contains the upper 8 bits of the 16-bit chip part number (3662). It is a read-only register with a constant value.

9.2.1.19. CHIP_ID_2

Address: 0x16

Bit	Bit Name	Type	Default	Description
7:0	CHIP_ID_2	RO	b' 00010000	Fixed configuration.

9.2.1.20. RESERVED

Address: 0x20

Bit	Bit Name	Type	Default	Description
7:0	RESERVED	RAZ	b'00000000	Reserved

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9.2.1.21. PORT1_RESET_CTRL

Address: 0x21

Bit	Bit Name	Type	Default	Description
7:1	RSVD	RAZ	b'0000000	Reserved.
0	PORT1_SOFT_RESET	R/W	b'0	This bit is self-clearing. Writing a '1' to this bit initiates a software reset, and the bit automatically clears to '0'. All read/write registers are reset to their POR default settings. Writing a '0' to this bit has no effect. Reads of this bit always return '0'.

This register is meant to initiate reset of the chip via I^2C write.

9.2.1.22. PORT1_LINK_CTRL1

Address: 0x22

Bit	Bit Name	Type	Default	Description
7:6	PORT1_SPEED_CTRL	RW	b'00	This bit field defines the POR default setting for the USB2.0 speed. 00: Manage the speed via Auto negotiation. 01: LS/FS only. 10: Reserved. 11: Reserved.
5:4	PORT1_ROLE_CTRL	RW	b'00	Determines the redriver role. 00: Dual role. Supports negotiation of eUSB2 port configuration for both host and device roles. This is the standard operating mode managed through eUSB2 exchanges initiated by the host. 01: Force Host role. When the bits are set to '01', the redriver is forced into the USB Host role, overriding any configuration commands received via eUSB2. However, the redriver still acknowledges configuration messages from the host. 10: Force Device role. When these bits are set to '10', the redriver is forced into the USB Device/Peripheral redriver role, overriding any configuration commands received via eUSB2. However, the redriver still acknowledges configuration messages from the host. 11: Reserved. The forced host/device role setting is applicable only when Link Control 1[2:0] bits are set to '2'.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT1_OPERATIONAL_MODE	RW	b'000	The bits define the operational mode of the redriver. 0: Auto negotiation on the link (mode determined via control messages and link negotiation). 1: Deep standby mode (eUSB2 pins are pulled down, USB2.0 pins are held in weak pull-down condition and I^2C register contents are preserved).

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				2: Connect detect state. Used to force the redriver into its the Connect. Detect state (refer to eUSB2 specification). The action takes effect only at the moment the register is written. If an overriding condition, such as RST_N = 0, exists, the write operation is discarded, even after the condition is cleared. In this scenario, the role control field (register 0x22) must have only one bit set. These bits specify the role the redriver should assume. This command directs the redriver to enter the corresponding the Connect.Detect state based on the role control setting. Once the state transition is complete, the redriver automatically responds to the eUSB2/USB2.0 bus conditions accordingly. 3: Compliance Mode (HS L0 condition). This action is equivalent to receiving the Control Message CM.Test, enabling the system to force the redriver into the HS.L0 state. The roles are determined by the role control bits. In this case, only a single bit must be set in the role control field; if both or neither bit is set, the command is ignored. 4 to 7: Reserved.

This register is used to force the redriver role and fix the operating speed.

9.2.1.23. PORT1_LINK_CTRL2

Address: 0x23

Bit	Bit Name	Type	Default	Description
7:2	RSVD	RAZ	b'000000	Reserved.
1	Auto Resume Enable	RW	b'0	0: Follow eUSB specification. 1: Enable Auto resume and asynchronous wake-up feature.
0	PORT1_FORCE_ESE1	RW	b'0	Bit to force Extended SE1 signaling. 0: No action. 1: Self-clearing bit. When written to 1, Redriver generates extended SE1 onto the eUSB2 pins. Typically, only the host redriver initiates this action upon detecting a HS disconnect. However, this feature enables the system to enforce an extended SE1 signaling state through the I^2C interface as required.

This register configures a specific feature of the redriver.

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9.2.1.24. PORT1_EUSB2_RX_CTRL

Address: 0x24

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT1 eUSB2 HS Rx Squelch Detection Threshold	RW	b'10	The bits set the squelch detector threshold level for transitioning from Low to High on eUSB2 HS signaling pins. 00: 50 mV. 01: 65 mV. 10: 85 mV. 11: 95 mV. All settings are within ±25 mV of the specified nominal values. The squelch detector incorporates a 10 mV hysteresis to enhance noise immunity.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT1 eUSB2 HS Rx Equalization	RW	b'000	The bits set the nominal eUSB2 receive equalization gain at 240 MHz relative to the DC gain. All settings are accurate within ±1 dB of the specified nominal values. 000: 0 dB. 001: 1 dB. 010: 2 dB 011: 3 dB. 100: 4 dB. 101 to 111: Reserved.

This register configures the eUSB2 receiver equalization and squelch detection threshold settings

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9.2.1.25. PORT1_EUSB2_TX_CTRL

Address: 0x25

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT1 eUSB2 HS Tx Output Swing	RW	b'01	The bits configure the output signal swing for high-speed (HS) signaling on the eUSB2 transmitter side when the interface is properly terminated. 00: 180 mV. 01: 200 mV. 10: 220 mV. 11: 240 mV. All settings are within ±40 mV of nominal value mentioned above.
3:2	RSVD	RAZ	b'00	Reserved.
1:0	PORT1 eUSB2 HS Tx De-emphasis	RW	b'00	The bits determine the Tx de-emphasis (nominal) level for HS signaling on eUSB2 pins. The de-emphasis duration is between 0.75 to 1 HS bit time. 00: 0 dB. 01: 1 dB. 10: 2 dB. 11: 3 dB. All settings other than '00' are within ±1 dB of nominal value mentioned above.

The register programs the eUSB2 transmitter output swing and de-emphasis level (applicable for high-speed signaling only).

9.2.1.26. PORT1_USB2_RX_CTRL

Address: 0x26

Bit	Bit Name	Type	Default	Description
7	RSVD	RAZ	b'0	Reserved.
6:4	PORT1 USB2.0 HS Rx Squelch Detection Threshold	RW	b'100	The 3 bits set the squelch detector threshold level for the Low-to-High transition in HS signaling on USB2.0 pins. 000: Reserved; not for use. 001: 65 mV. 010: 85 mV. 011: 95 mV. 100: 110 mV. 101: 125 mV. 110: 140 mV. 111: 155 mV.

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				All settings are within ±25 mV of nominal value mentioned above Squelch detector implements hysteresis of 10 mV to improve noise immunity.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT1 USB2.0 HS Rx Equalization	RW	b'000	The 3 bits configure the nominal USB2.0 receive equalization gain at 240 MHz relative to the DC gain. All settings are accurate within ±1 dB of the specified nominal values. 000: 0 dB. 001: 1 dB. 010: 2 dB. 011: 3 dB. 100: 4 dB. 101 to 111: Reserved.

This register configures the eUSB2 receiver equalization and squelch detection threshold settings.

9.2.1.27. PORT1_USB2_TX_CTRL1

Address: 0x27

Bit	Bit Name	Type	Default	Description
7:6	RSVD	RAZ	b'00	Reserved.
5:4	PORT1 USB2.0 HS Tx De-emphasis Bit Duration	RW	b'10	The bits configure the de-emphasis bit time (UI) for HS signaling on the USB2.0 Tx side. 00: 0. 01: 0.5 UI. 10: 0.8 UI. 11: Reserved. All settings are within ±0.2 UI of nominal value mentioned above.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT1 USB2.0 HS Tx De-emphasis	RW	b'010	The bits determine the Tx de-emphasis (nominal) level for HS signaling on USB2.0 pins. 000: 0 dB. 001: 1 dB. 010: 2 dB. 011: 3 dB. 100: 4 dB. 101: 5 dB. 110: 6 dB. All settings other than '000' are within ±1 dB of nominal value mentioned above.

This register configures the transmit-side parameters, including de-emphasis levels for the USB2.0 side.

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9.2.1.28. PORT1_USB2_TX_CTRL2

Address: 0x28

Bit	Bit Name	Type	Default	Description
7	RSVD	RAZ	b'0	Reserved.
6	PORT1 USB2.0 FS Rise/Fall Time	RW	b'1	This bit controls the rise and fall times of the FS Tx driver on the USB2.0 pins. 0: 8 to 20 ns. 1: 4 to 14 ns. Load conditions are as defined in USB standard.
5:4	PORT1 USB2.0 HS Rise/Fall Time	RW	b'10	The 2 bits define the Tx driver slew rate for HS signaling on the USB2.0 pins. 00: 500 to 900 ps. 01: 400 to 830 ps. 10: 300 to 760 ps. 11: Reserved. Load conditions are as defined in USB standard.
3	RSVD	RAZ	b'0	Reserved.
2:0	PORT1 Tx Output Signal Swing	RW	b'011	The 3 bits specify the Tx output signal swing level for HS signaling on USB2.0 pins (when the interface is terminated). 000: 350 mV. 001: 400 mV. 010: 450 mV. 011: 500 mV. 100: 550 mV. 101: 600 mV. 110: 650 mV. 111: 700 mV. All settings are within ±10% of nominal value mentioned above.

This register configures the transmit-side settings, including the Tx output driver slew rate and output signal swing on the USB2.0 side.

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9.2.1.29. PORT1_USB2_HS_TERM

Address: 0x29

Bit	Bit Name	Type	Default	Description
7:3	RSVD	RAZ	b'00000	Reserved.
2:0	PORT1 USB2.0 HS Termination Control	RW	b'010	The bits set the HS termination on USB2.0 pins, defining the differential impedance. 000: 100 Ω differential. 001: 95 Ω differential. 010: 90 Ω differential. 011: 85 Ω differential 100: 80 Ω differential. 101 to 111: Reserved. All settings are within ±10% of nominal value mentioned above.

This register configures the HS termination values on the USB2.0 pins.

9.2.1.30. PORT1_USB2_DISCONNT_TH

Address: 0x2A

Bit	Bit Name	Type	Default	Description
7:2	RSVD	RAZ	b'000000	Reserved.
1:0	PORT1 HS Disconnect Threshold Level	RW	b'00	The bits determine the HS Disconnect detector threshold level on USB2.0 pins. 00: 575 mV. 01: 675 mV. 10: 775 mV. 11: 875 mV. All settings are within ±50 mV of nominal value mentioned above. The detector implements hysteresis of 30 mV to improve noise immunity.

This register configures the HS disconnect threshold level on the USB2.0 pins.

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9.2.1.31. PORT1_DEVICE_STATUS

Address: 0x2B

Bit	Bit Name	Type	Default	Description
7:4	RSVD	RAZ		Reserved.
3:2	PORT1 Speed of Operation Status	RO		The bits show the current state of redriver speed of operation. 00: LS. 01: FS. 10: HS.
1:0	PORT1 Redriver Role	RO		The bits show the current role played by the redriver. 00: No role determined yet. 01: Device side redriver. 10: Host side redriver.

This register reflects the current state of the redriver functionality. It is a read-only register; any write operation has no effect.

9.2.1.32. PORT1_LINK_STATUS

Address: 0x2C

Bit	Bit Name	Type	Default	Description
7:3	RSVD	RAZ		Reserved.
2:0	PORT1 Device Link Status	RO		The status bits reflect the device and link state. 000: Deep standby. 001: Connect detect. 010: L1. 011: L2. 100: Active LS/FS (L0) 101: Active HS (L0). 110: Active HS (L0) forced due to USB2.0 compliance mode. 111: This setting represents transitioning condition between different states (For example: Suspend to Resume to L0).

This status register reflects the current state of the redriver device and link. It is read-only, and write operations have no effect.

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9.2.1.33. PORT1_RAP_SIGN

Address: 0x2D

Bit	Bit Name	Type	Default	Description
7:0	PORT1 RAP_Signature	RW	b'00000000	0x00: No RAP Access to DIO36620 I^2C Registers. 0x37: RAP allowed read only access to Status, REVISION_ID, and Chip ID registers. 0x92: RAP allowed read only access to I^2C customer registers. 0x21: RAP allowed write/read access to I^2C customer registers. All others: No RAP Access to registers.

The RAP signature controls and restricts RAP command access to the redriver's registers.

9.2.1.34. PORT1_VDX_CTRL

Address: 0x2E

Bit	Bit Name	Type	Default	Description
7:1	RSVD	RAZ	b'0000000	Reserved.
0	PORT1_VDX_ Control	RW	b'0	VDX Control - Host Side Redriver Function. 0: Disable VDX_SRC. 1: Enable VDX_SRC. The host must enable VDX_SRC within 200 ms after a disconnect, and the DIO36620 VDX_SRC circuitry is automatically disabled upon detection of the next connection.

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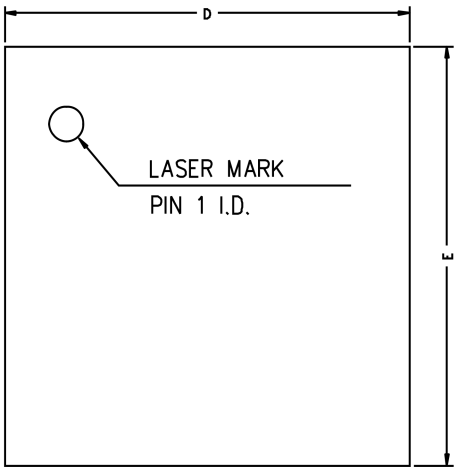
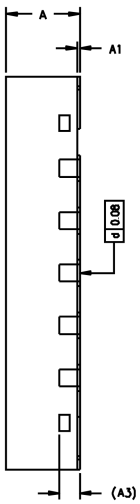
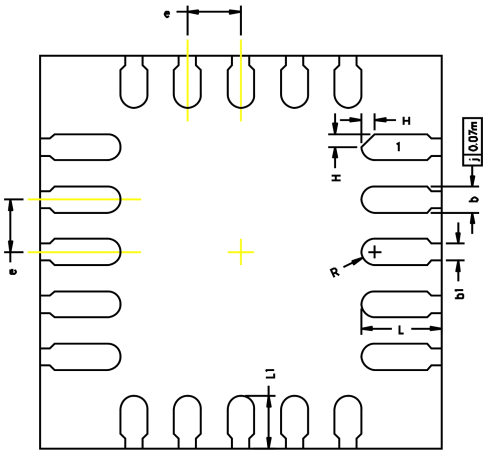
10. Physical Dimensions: QFN3×3-20



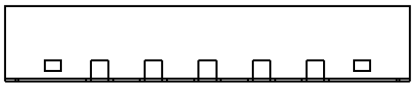
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
b1		0.13 REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.35	0.40	0.45
H		0.10 REF	
R		0.10 REF	
L	0.50	0.60	0.70
L1	0.30	0.40	0.50

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